A 0.16nJ/bit/iteration 3.38mm^2 Turbo Decoder Chip for WiMAX/LTE Standards

Cheng-Hung Lin
Department of Electrical Engineering
Yuan Ze University
Jungli 320, Taiwan

Chun-Yu Chen
Silicon Motion Technology Corp.
Sindian 231, Taiwan

En-Jui Chang, and
An-Yeu (Andy) Wu
Graduate Institute of
Electronics Engineering,
National Taiwan University,
Taipei 106, Taiwan

Abstract—**This paper presents a turbo decoder chip design supporting distinct convolutional turbo code schemes in WiMAX and LTE systems. A contention-free vectorizable dual-standard interleaver is proposed to enhance the hardware utilization. Moreover, a warm-up free parallel MAP decoding is proposed to improve the throughput rate. The overall VLSI architecture of the proposed CTC decoder is presented for supporting the WiMAX/LTE systems. This chip fabricated in a core area of 3.38 mm^2 by 90nm CMOS process is measured at 152 MHz with a power consumption of 148.1 mW and a throughput rate of 186.1 Mbps. This chip achieves a high area efficiency of 0.36 bit/mm^2 and a low energy efficiency 0.16 nJ/bit/iteration.**

Keywords- WiMAX, LTE, Multi-standard, Turbo Decoder.

I. INTRODUCTION

Recently, convolutional turbo codes (CTCs) have been regular schemes for wireless communications in order to have a reliable transmission over noisy channels. The single-binary (SB) CTC proposed in 1993 [1] was adopted in LTE because of its coding gain close to the Shannon limit. The non-binary CTC proposed in 1999 [2] was introduced to have a superior coding performance than the SB-CTC. The double-binary (DB) CTC was adopted in WiMAX.

To deal with the different data rates and CTC schemes, the multi-standard CTC decoder which works across the multiple standards of wireless WANs can enable smooth migration for different multimedia applications within a same device. The prevalent sliding-window (SW) maximum *a posteriori* algorithm (MAP) deals with variant CTC blocks with intrinsic low throughputs [3]. Thus, to support high-throughput CTC decoding for future wireless WAN systems, a parallel decoding architecture which embeds multiple MAP decoding kernels is inevitable. The parallel decoding architecture may encounter memory contention for parallel interleaved data access. Especially for the multiple-standard CTC interleaving, the memory contention occurs frequently and needs to be solved to make the parallel MAP decoding realizable.

In this paper, a contention-free parallel decoding architecture for WiMAX/LTE CTC decoding is proposed in Section II. Contention-free parallelisms for WiMAX/LTE CTC interleaving are analyzed and a parallel vectorizable WiMAX/LTE CTC interleaver is proposed. In addition, a warm-up free parallel MAP decoding is proposed to achieve the throughput rates of WiMAX and LTE systems. In Section III, the proposed CTC decoder for the WiMAX/LTE standards has been fabricated in a core size of 3.38 mm^2 by using UMC 90nm CMOS technology. This prototyping chip supports all 17 modes of the WiMAX CTC scheme and selected 18 modes of the LTE CTC scheme. The throughput rate of 186.1 Mbps is maximally measured at 152 MHz with a power consumption of 148.1 mW. Finally, the concluding remarks are given in Section IV.

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II. PROPOSED CTC DECODER FOR WIMAX/LTE STANDARDS

A. Contention-free Vectorizable Dual-standard Parallel Interleaver

For parallel decoding, multiple MAP kernels may read/write a same memory bank simultaneously. Since the port of a memory is finite, this simultaneous memory access needs to be prohibited. Without a cautious analysis of the dual-standard CTC interleaving, the memory contention occurs frequently and makes the parallel MAP decoding unrealizable for an unexpected parallelism.

For a hardware design of the parallel interleaving, the solution to memory contention has been discussed in [4]. The interleaver is contention-free when the interleaving sequence $\Pi(t)$ satisfies

$$\left\lfloor \frac{\Pi(t+jW)}{W} \right\rfloor \neq \left\lfloor \frac{\Pi(t+kW)}{W} \right\rfloor , \quad (1)$$

where N is the decoding block size, W is the basic windows size, P is the parallelism of the parallel MAP decoding ($N = PW$), $0 \leqq t < W$, and $0 \leqq j, k < P$. The terms on both sides of (1) are indices of the memory banks that are accessed by the j^{th} and k^{th} MAP kernels at the t^{th} time instant. This inequality need to be true for any time instant t for no memory contention.

For an interleaver design, the complexity of the interleaving address generation is also critical. Each physical memory bank requires an address decoder to transform the global interleaving address to the local address for each memory bank. As the parallelism P increases, the duplication of address decoder leads to hardware inefficiency. A better solution is to use the same address for all memory banks. This property requires the

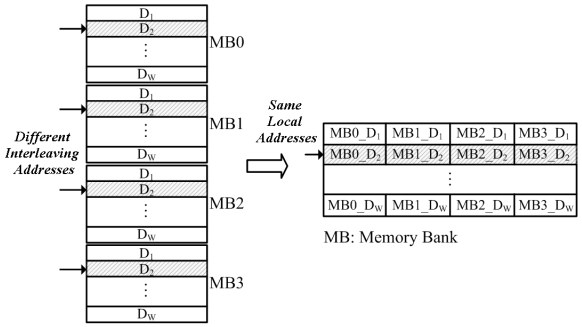

Figure 1. Vectorizable interleaving address for memory banks.

TABLE I. AVAILABLE PARALLELISM FOR WIMAX /LTE SYSTEMS.

LTE (Selected 18 modes)		WiMAX (all 17 modes)	
N	Available parallelism	*N*	Available parallelism
48	1 2	24	1
72	1 2 3	36	1
96	1 2 3 4	48	1 2
144	1 2 3 4 6	72	1 2 3
192	1 2 3 4 6 8	96	1 2 3 4
216	1 2 3 4 6 8 9	108	1 3
240	1 2 3 4 5 6 8 10	120	1 2 3 4 5
288	1 2 3 4 6 8 9 12	144	1 2 3 4 6
360	1 2 3 4 5 6 8 9 10 12 15	180	1 2 3 4 5 6
384	1 2 3 4 6 8 12 16	192	1 2 3 4 6 8
432	1 2 3 4 6 8 9 12 16 18	216	1 2 3 4 6 8 9
480	1 2 3 4 5 6 8 10 12 15 16 20	240	1 2 3 4 5 6 8 10
960	1 2 3 4 5 6 8 10 12 15 16 20	480	1 2 3 4 5 6 8 10 12
1920	1 2 3 4 5 6 8 10 12 15 16 20	960	1 2 3 4 5 6 8 10 12
2880	1 2 3 4 5 6 8 9 10 12 15 16 18 20	1440	1 2 3 4 5 6 8 9 10 12
3840	1 2 3 4 5 6 8 10 12 15 16 20	1920	1 2 3 4 5 6 8 10 12
4800	1 2 3 4 5 6 8 10 12 15 16 20	2400	1 2 3 4 5 6 8 10 12
6144	1 2 3 4 5 6 8 12 16	-	-

interleaving address to satisfy

$$\Pi(t + jW) \bmod W = \Pi(t) \bmod W, \qquad (2)$$

where $0 \leqq t < W$, and $0 \leqq j < P$. The equality implies that each MAP kernel access data based on the same local address. Based on this vectorizable property, only one set of address generator is required. All memory banks can merge into a single physical memory with data stored and fetched as vectors as shown in Fig. 1.

A high-level simulation model for (1) and (2) is used to analyze the available parallelism for the LTE and WiMAX standards with $24 \leqq W \leqq 36$. The details of WiMAX and LTE CTC interleaving can be referred to in [5] and [6], respectively. The available parallelism achieving the contention-free and vectorizable interleaving address is shown in Table I and we choose $P = 8$ for the proposed VLSI architecture of WiMAX/LTE CTC decoder. Fig. 2 shows the proposed contention-free vectorizable dual-standard parallel interleaver and the CTC controller. The CTC controller provides control signals and initial parameters. To perform the radix-4 SB/DB EML-MAP decoding [7], the proposed dual-standard address generators generate the WiMAX addresses or the radix-4 LTE even addresses by adopting a hardware sharing technique. The additional LTE address generators generate the radix-4 LTE odd addresses in the LTE modes. The LTE and WiMAX interleaving parameters ($P0$, $TP1$, $TP2$, $TP2$, $P(0)$, $H(0)$, $J(0)$, and f_2) can be implemented in a look-up table. The address

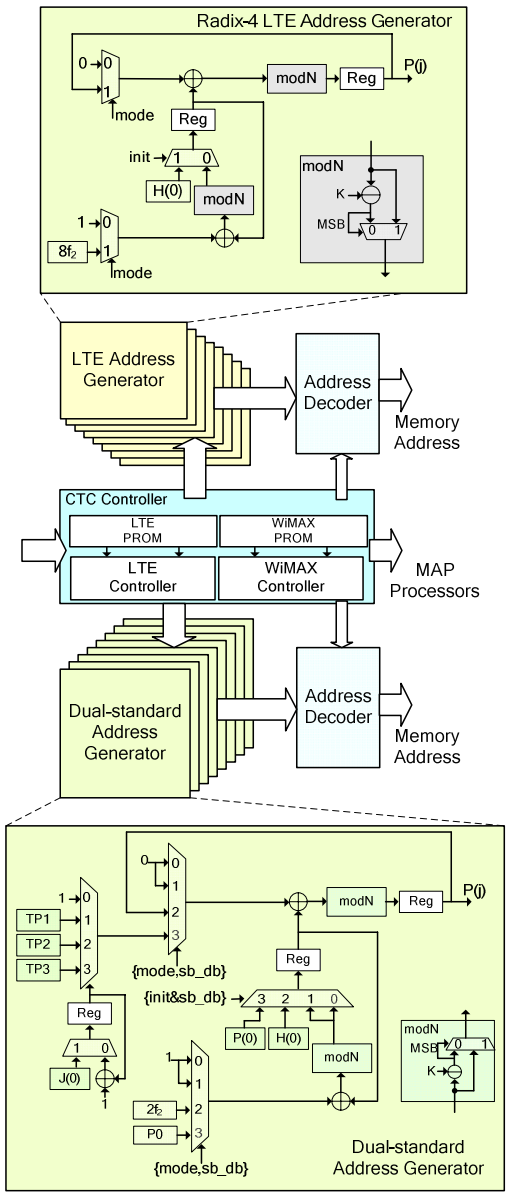

Figure 2. Block diagram of the WiMAX/LTE parallel interleaver and CTC controller.

decoder transforms the interleaving addresses into the contention-free addresses of the memory subbanks.

B. High-throughput Warm-up Free Parallel MAP Decoding

The SW MAP decoding was proposed to facilitate the memory cost of CTC decoders. However, the SW MAP decoding deals with any CTC frame size but has intrinsic low throughputs. The hybrid-window (HW) MAP decoding described in [7] applies parallel MAP kernels to decode one received block. Because of the warm-up processes of forward states metrics, the decoding latency is prolonged to $4W$. Nevertheless, the HW MAP decoding can shorten the decoding cycles to $N/P + 4W$ by working with several sub-blocks simultaneously.

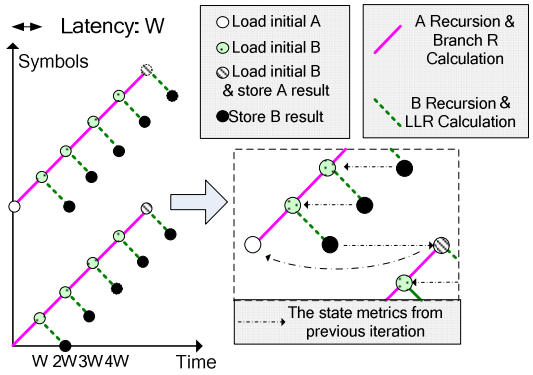

Figure 3. The warm-up free hybrid-window (HW) MAP decoding.

In this paper, a warm-up free HW MAP decoding is proposed to further reduce the decoding latency. The timing chart is shown in Fig. 3. Instead of performing a warm-up recursion, each MAP kernel achieves the initial state metrics (both A and B in Fig. 3) by fetching the state metrics of previous iteration from the border metrics memory (BMM). The loss of coding gain is less than 0.03 dB at BER of 10^{-5}. The decoding latency can be reduced to one W. Compared to the HW MAP decoding in [9] with P = 8, W = 24, and the radix-4 decoding, the throughput rates can be improved 60% for N = 48 and 15% for decoding the N = 6144.

C. *Proposed CTC Decoder for WiMAX/LTE Systems*

Fig. 4 shows the VLSI architecture of the proposed CTC decoder for WiMAX/LTE systems with P = 8. For verifying the proposed design techniques, this prototyping decoder supports all 17 modes of the WiMAX CTC scheme and selected 18 modes of the LTE CTC scheme. The proposed WiMAX/LTE parallel interleaver generates addresses for the input memories and extrinsic memories so that the normal-order or interleaved-order values can be processed between the 8 warm-up free HW MAP kernels and the memory subbanks. The number of active MAP kernels with the distinct design modes is shown in Table II. The computational modules and storages of the radix-4 SB/DB EML-MAP decoding in [8] ware applied to the MAP kernels to achieve a high area usage. Moreover, the radix-4 traceback structure in [7] was adopted to reduce the area and power of the state metric cache. Because of the radix-4 SB MAP decoding, two extrinsic information values are accessed in parallel. The bit-level extrinsic information exchange [9] was also adopted to make the extrinsic buffer access only two extrinsic information values for the radix-4 DB MAP decoding. Thus, the extrinsic buffer for the radix-4 SB/DB MAP decoding can be fully shared. When the targeted iteration number is reached or the hard bits of two half iteration are the same, the CTC decoder finishes the decoding procedure and outputs the hard bits from the output memories.

III. Experimental Results

The proposed CTC decoder has been implemented in an ASIC by using Verilog HDL codes synthesized with the standard cell library of UMC 90nm CMOS process. The design of the CTC decoder is simulated using C-to-RTL flow. The

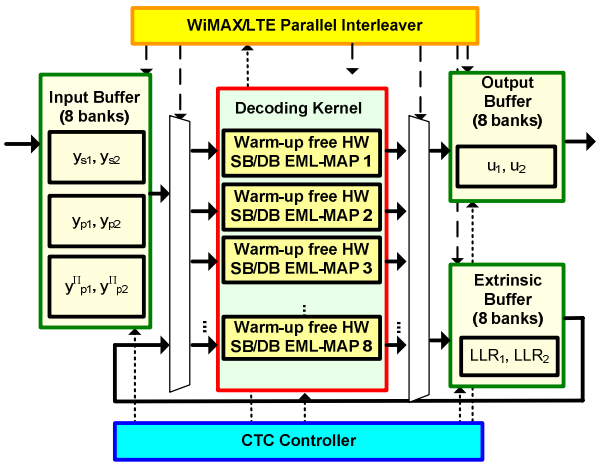

Figure 4. Block diagram of the proposed CTC decoder for WiMAX/LTE standards.

TABLE II. DESIGN MODES OF THE PROPOSED CTC DECODER.

Mode		Info. Bits	Active MAPs	Mode		Info. Bits	Active MAPs
WiMAX	LTE			WiMAX	LTE		
1	18	48	1	10	27	384	8
2	19	72	1	11	28	432	8
3	20	96	2	12	29	480	8
4	21	144	2	13	30	960	8
5	22	192	4	14	31	1920	8
6	23	216	3	15	32	2880	8
7	24	240	4	16	33	3840	8
8	25	288	4	17	34	4800	8
9	26	360	6	-	35	6144	8

quantization parameters are the same to Table III in [8] met the targeted BER of 10^{-5} for WiMAX and of 10^{-3} for LTE. Fig. 5 shows the BER performance of the distinct CTC schemes decoded by the CTC decoder based on AWGN channels and 6 iterations. The proposed CTC decoder chip has been fabricated in a die area of 7.18 mm^2 and a core area of 3.38 mm^2. The total gate count of the proposed contention-free parallel interleaver and CTC controller is 30.4 Kgates. The decoder contains 232.8 Kb RAM. Fig. 6 shows the chip layout and die photo of the prototyping CTC decoder chip. The prototyping chip is fabricated and maximally measured at 152 MHz operating frequency at core supply voltage of 1.1 V. In order to consider reduction of power consumption, the core supply voltage is reduced to form 1.1 V to 0.9 V. The measured maximal operating frequencies and power consumptions are shown in Fig. 7.

For the maximum block size in WiMAX (Mode 17 in Table II), the a throughput rate is 178.4 Mbps (@152 MHz, 6 iterations). For the maximum block size in LTE (Mode 35 in Table II), the chip achieves a throughput rate of 186.1 Mbps with a power consumption of 148.1 mW (@152 MHz, 6 iterations). The comparison of our decoder and other works are shown in Table III. For supporting the both WiMAX and LTE CTC decoding, this chip achieves a high area efficiency of 0.36 bit/mm^2 with a low energy efficiency of 0.16 nJ/bit/iteration.

IV. Conclusion

The fabricated CTC decoder chip for WiMAX/LTE standards employs the proposed contention-free vectorizable

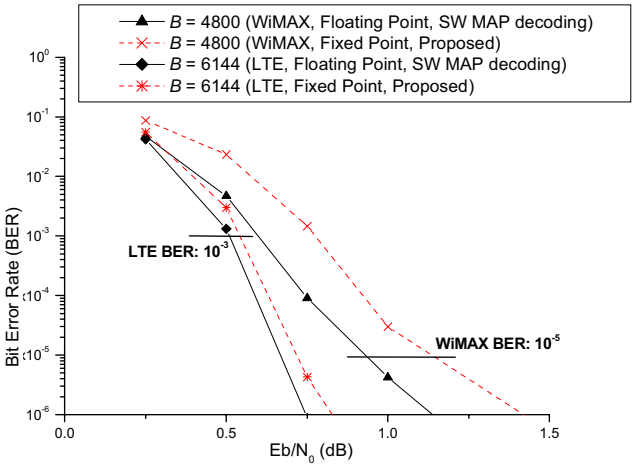

Figure 5. BER performance of the coderate-1/3 CTC decoding by using the prototyping CTC decoder chip.

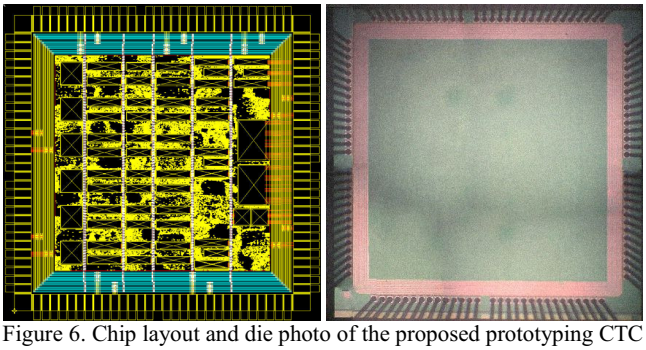

Figure 6. Chip layout and die photo of the proposed prototyping CTC decoder chip.

dual-standard CTC parallel interleaver and high-throughput warm-up free HW MAP decoding. This chip is the dual-standard CTC decoder to meet the both WiMAX and LTE data-rate requirements with a high area efficiency of 0.36 bit/mm^2 and a low energy efficiency 0.16 nJ/bit/iteration.

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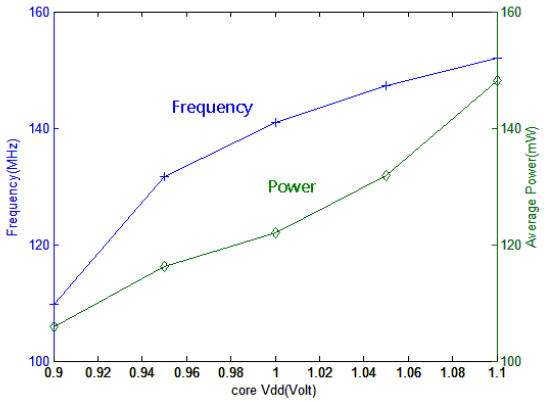

Figure 7. Measured frequency and power of the proposed CTC decoder chip.

TABLE III. COMPARISONS OF THE CTC DECODER CHIPS.

	[3]	[10]	[6]	[11]	Proposed
Technology	0.13 µm	0.13 µm	90 nm	0.13 µm	90 nm
Core Voltage	1.2 V	1.2 V	1 V	1.2 V	1.1 V
Standard	UMTS, HSDPA	Mobile WiMAX	LTE	LTE, WiMAX	LTE, WiMAX
Max. info. bits	5144	4800	6144	6144	6144
MAP	Radix-2 SB	Radix-4 DB	Radix-2 SB	Radix-4 SB/DB	Radix-4 SB/DB
Parallel MAP #	1	1	8	8	8
Max. Frequency (MHz)	246	200	275	250	152
Core Area (mm^2)	1.20	2.24	2.10	10.7	3.38
Max. Throughput T (Mbps)	20.2	48.5	129	187.5	186.1
Power (mW) @ T	57.8	N/A	2.0	N/A	148.1
EE [1] (nJ/bit/iter.)	0.70	N/A	0.14	0.61	0.16
AE [2] (bit/mm^2)	0.06	0.11	0.22	0.11	0.36

[1] Energy efficiency (EE) = Power / (Throughput Rate × Iteration).
[2] Area efficiency (AE) = Throughput Rate / (Core Area × Frequency).

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