High Performance Adaptive Routing for Network-on-Chip Systems with Express Highway Mechanism

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Abstract—The Network-on-Chip (NoC) offers flexible and scalable communication architecture for many-core systems in the future. The routing algorithm dominates the system performance with more complicated communication and scaling. However, with the amount of processors increasing, congestion happened easily when most of the processors need to access the memory. In order to solve processor-memory accessing problem, in this paper, we propose heterogeneous-network architecture with Highway selection strategy. Our experiments show that the proposed one exceeds the performance of conventional adaptive routing under different traffic scenarios with 56.63% maximum latency reduction and have better scalability in larger scale NoC.

Keywords—Network-on-Chip; adaptive routing; memory access; express topology

I. INTRODUCTION

With the growth of semiconductor technology, System-on-Chip (SoC) design heads to a high-density on-chip components integration [1]. Network-on-Chip (NoC) architecture has been regarded as a method to achieve the performance. However, if certain component has been accessed frequently in NoC architecture, the on-chip traffic load becomes congested and leads to huge latency degradation in the network system.

The severe traffic congestion appears commonly in a hybrid multiprocessor-memory network [2]. Fig. 1(a) shows that numerous processors access the same share memory repeatedly results in the traffic imbalance in the network, called Hotspot traffic. Unfortunately, Hotspot traffic degrades the overall system performance owing the congested traffic around share memory. Therefore, to overcome the problem of Hotspot traffic, an effective network architecture and packet routing method are critical for high-performance NoC [3]. To increase the efficiency of data transmission, the virtual-channel express topology architecture was proposed in NoC system [4]. By using heterogeneous reduced pipeline routers, it can bypass buffering and arbitrations to reduce the packet latency.

To further reduce congestion between hotspot nodes in the hybrid multiprocessor-memory network, we follow the design concept of highway system and propose highway-based NoC for high-speed communication. Routing algorithms determine the path from source to destination that a packet should be transmitted through. It consists of two major parts: 1) Routing function chooses a set of output candidates based on certain turn model [5].

2) Selection function makes a choice in the set of output candidates to select the best output channel based on network information. Therefore, in this paper, to effectively utilize the proposed highway and regulate traffic flow in NoC, we present an adaptive routing with a selection strategy based on the liquidity of highway traffic.

In summary, this paper proposes Highway-based NoC Scheme, which consists of H-tree highway architecture and highway traffic-aware adaptive routing algorithm. The main contributions of this paper include the following:

- **H-tree Highway Architecture**: Shown in Fig. 1(b), H-tree based infrastructure had been proved for balancing traffic load effectively [6], and it would mitigate the traffic around share memory. Furthermore, we construct a virtual express architecture in our proposed highway scheme.

- **Highway Traffic-Aware Adaptive Routing Algorithm**: We consider the liquidity of buffer space on highway and the location of destination to select the best path. Our contribution is to further improve the routing performance comparing to conventional routing algorithm under Hotspot traffic, also provides a better scalability. Furthermore, the router architecture is designed and evaluated.

II. RELATED WORKS AND BACKGROUND

In this section, we review the concept of express topologies includes physical express and virtual express architecture. Also, in order to compare with conventional methods, relevant selection functions in adaptive routing algorithm are discussed.
A. Express Topology in 2-D mesh NoC architecture

A NoC baseline router typically has 4-stage pipeline, including 1) VA: incoming packets get buffered and arbitrating for the next router, 2) SA: connecting all the input to the output by crossbar, 3) LT: winning the switch traverse the crossbar, and 4) ST: push the packets to the output channel [4]. It leads to poor scalability owning to the long hop-to-hop latency. Thus, there are several previous works that advocate for packets transmitted in a long distance to bypass the intermediate routers. We can classify these works into two categories. 1) Physical Express Topologies (PET): adding physical channels to skip intermediate routers. 2) Virtual Express Topologies (VET): modified the pipeline router where certain stages are skipped to bypass the router virtually. These two express topologies could improve the network throughput significantly. We choose VET as our scheme for its high throughput with feasible cost.

B. Selection Functions in Adaptive Routing Algorithm

In order to mitigate traffic congestion and improve average throughput in the network, selection function provides a mechanism which chooses the best output channel from a sets of candidates selected by adaptive routing functions. Selection function takes the current network information into account to determine which channel is better. For example, some algorithm may consider spatial network information, such as the remaining free-slots in the next hop router, called Output channel Buffer-Level (OBL) [7]. Another one considers the buffer spaces of routers that are two hops away, scoring all the output channel and choosing the best one, called Neighbor-on-Path (NoP) [8]. The other congestion-avoided selection algorithm like, Regional Congestion Awareness (RCA) [9], and Dynamic Bandwidth Estimation (DBE) were proposed which based on the local information [10]. Considering hardware cost and performance, we choose NoP as our baseline selection.

However, the works mentioned above are congestion-aware algorithms which aim at balancing the overall network traffic load. To the best of our knowledge, only few researches have considered about multiprocessor-memory access issue to prevent traffic congestion on certain router. The concept of virtual express architecture is to mitigate the high-intensity traffic load around the on-chip share memory. Therefore, our motivation is to avoid congestion by constructing heterogeneous network architecture and considering the liquidity of buffer space on the highway as a new NoC strategy.

III. HIGHWAY-BASED ADAPTIVE ROUTING ALGORITHM

We have discussed that congestion-aware selection algorithms may restrict the performance under multiprocessor-memory access issue. In this section, we propose the H-tree highway-based adaptive routing algorithm and classify into two parts in the following discussion.

A. H-tree Highway Architecture

By the inspiration of transportation system in real life, we attempt to mitigate the traffic load around share memory by similar situation happened in the capital of a country. Therefore, we construct bidirectional H-tree architecture at the center of the network as the concept of highway system. In order to balance the network traffic, we divide the network into quarters and set the boundary at the first quarter and the last quarter from top as well as left. Moreover, as shown in Fig. 2(a) (b), we choose Odd-Even turn model as our baseline routing function, the constraint of Odd-Even routing function limits the packets on certain turn. They are not allowed to make a East-to-North (EN) or NW turn on even column, neither to make an ES or SW turn on odd column. To utilize every turn equally, we build a bidirectional Highway to permit both directional transmissions. For example, as shown in Fig. 2(c), in an 8x8 mesh topology, we set (2, 2), (5, 2), (2, 5), (5, 5) as the boundary of highway and (3, 2), (4, 2), (3, 3), (4, 3), (3, 4), (4, 4), (3, 5), (4, 5) as the bidirectional highway.

Fig. 2. The Odd-Even turn model in (a) even column and (b) odd column; (c) example of transmission from source to destination limited by Odd-Even routing function.

After constructing overall architecture, we need to modify the highway router. Virtual Express Topologies provide a bypass expressway virtually to transmit packets in a rapid rate. Fig. 3 shows the comparison between the resident router and highway router. In Fig. 3(a), the resident router has 4 pipeline stages to transmit from input buffer to output channel. On the other hand, the packet transmitted proceeds to the switch traversal and forward without the buffering and allocation stage to reduce the pipeline latency in highway router, which is shown in Fig. 3(b).

Fig. 3. Comparison between (a) conventional transmission and (b) highway-based reduced pipeline transmission.Where VA: VC Allocation; SA: Switch Allocation; ST: Switch Traversal; LT: Link Traversal.

Although it only takes 2 stages passing the packet through each highway router, it takes 4 stages to transmit a packet from resident to highway router which leads to stall the highway performance. Fig. 4(a) shows that wormhole switching guarantees the integrity of each packet so that overall transmitting latency will not improve owning to the stall
To make use of Virtual Express Topologies efficiently, we go deeper into small data granularity which called flit-level interleaving [12]. As shown in Fig. 4(b), it allows header flit of two different packets to reserve the same output channels simultaneously on each highway router and transmit flits of both packets alternately. That is to say, the highway router keep transmitting the other packet rather than waiting for the same packet for every 4 cycles.

Fig. 4. Comparison between (a) conventional wormhole switching and (b) flit-level interleaving.

Finally, when a local processor wants to access the shared on-chip memory at the center of the network, it could take advantage of the reduced pipeline highway router with flit-level interleaving to transmit the packet in a rapid speed.

B. Highway Traffic-Aware Adaptive Routing Algorithm

Nevertheless, we should limit the amounts of packets that can be transmitted through highway because large amounts of packets would lead to congestion on highway. The formula according to the discussion above is as follow,

\[ \text{Latency}_{\text{Overall}} = \text{Latency}_{\text{Traffic}} + \text{Latency}_{\text{Congestion}} = H \times R + T_c \]  

Where \( H \) represents hop counts from source to destination; \( R \) is the pipeline stage which could be classified into two types: 1) highway router contains two stages, and 2) resident router contains four stages. \( T_c \) stands for the congestion delay time. Considering the path from source to destination, a larger hop counts could result in longer traffic latency. On the other hand, a resident router consists of four stages pipeline comparing to highway router, which only has two stages to transmit a packet. That is to say, the problem we encounter is changed to how to distribute the traffic load between two different routers. We only allow the packet whose destination is on the highway to be transmitted through highway. This situation is like a multiprocessor-memory system, we assume the share on-chip memory is at the center of the network, and the packet can fully access the memory with highway to avoid congestion.

Besides, the more processors access the memory, the serious the congestion latency around the share memory is. In order to prevent congestion occurred without controlling the access from the processors, we examine the liquidity of the buffer space on the highway. It is allowed to utilize highway only when the buffer spaces on the highway are increasing or holding, which defines the liquidity.

The overview of highway is shown in Fig. 5. We check the following three conditions in order to control the amounts of packet passing through highway: 1) destination on highway, 2) the liquidity on highway, 3) the candidate chosen by routing function to highway direction. We would select the path by NoP when one of the three conditions fails.

Fig. 5. Overview of Highway Traffic-Aware Adaptive Routing Algorithm.

IV. PERFORMANCE EVALUATION

The experiments are evaluated by the NoC simulator, Noxim [13], which is an open source SystemC simulator. It uses wormhole switching mechanism and matrix arbitration. We use \( 8 \times 8 \) mesh topology network and the Odd-Even adaptive routing function to conduct the simulations under several traffic scenarios, including, Random, Shuffle, Bit reversal and Hotspot traffic. Under Hotspot traffic, packets would transmit to central router for 20% overhead which is similar to multiprocessor-memory access scheme.

Also, each channel has an input buffer with the size of 4 flits and each packet has 4 flits. For every run of simulation, the executed simulation is 12,000 cycles, with 2,000 warm-up cycles on the NoC system. The average latency and saturation throughput under different packet injection rate (pir) is the performance metric of each experiment.

A. Improvement in Saturation Throughput

We choose pir to achieve the saturation throughput. The definition of the saturation throughput is where average latency equals to twice of the zero-load latency [14].

The experiment result is shown in Fig. 6; it shows that Highway is superior to the other conventional selection functions from 40.18% to 53.65% under Hotspot traffic. Also, Highway outperforms OBL and NoP under the other three traffic scenarios as shown in the Table I.
B. Performance of Scalability

We analyze the scalability of Highway in performance by examining the network throughput under various topology sizes. The network throughput is defined as the saturation throughput multiplies the network nodes. The experiment result is shown in Fig. 7. With the growth of the topology size, the throughput of NoP and OBL would saturate around 0.8. However, the proposed work would enhance the performance from 1.4x to 1.75x comparing to the other selection functions.

C. Statistical Traffic Load Distribution (STLD)

On the other hand, Fig. 8(a) (b) shows the occupied buffer space in each router, which means congestion occur seriously with NoP while Highway does not. Also, STLD is shown in Fig. 8(c) (d). Highway can undertake larger traffic load than NoP under the same packet injection rate.

D. Hardware Evaluation

The highway router architecture contains two additional tables for flit-level interleaving and a liquidity control unit. 1) ID State Table: with 1 bit for current ID State; 2 bits for new and old id number and 4 bits for each input channel. 2) Forwarding Table: with 1 bit for current ID State; 1 bit for old id number and 4 bits for each output channel.

Furthermore, in order to detect the liquidity on highway, we need a control unit to examine the change rate with the previous one. Also, it costs 1 bit wire connecting to each router to limit the amount of packets to highway.

Table II reports the summary of the router area cost, which is programed by Verilog HDL and synthesized with standard cell library of UMC 90 nm CMOS process. The result shows that highway router has only 0.3% overhead compared with NoP scheme.

V. CONCLUSION

In this paper, we propose Highway routing algorithm that adopt the concept of expressway system under heterogeneous architecture to achieve better performance. The experiment results also demonstrate an improvement comparing to conventional routing algorithm with 56.63% maximum latency reduction. On the other hand, our proposed algorithm has better scalability and superior STLD performance compare to other adaptive selection functions.

REFERENCES