A Triple-Mode MAP/VA IP Design for Advanced Wireless Communication Systems

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***Abstract*—In this paper, a triple-Mode MAP/VA IP for advanced wireless communication Systems is implemented in 0.18μm CMOS process. We employ triple-mode MAP/VA timing charts that can run two different algorithms at the same time by complementing the idle time of each other. In order to conform to the advance communication standard, our IP can also perform as a reconfigurable trellis decoder. For WCDMA standard, this IP can operate at clock frequency of 100 MHz and achieve throughput rate of 4.17Mbps@6 iterations for turbo decoding and 1.56Mbps for convolutional decoding in concurrent MAP/VA mode from the worst-case static timing analysis and post-layout simulation.**

I. INTRODUCTION

In recent *forward-error-control coding* (FEC) systems, the convolutional decoder based on the *Viterbi algorithm* (VA) is a maximum-likelihood decoding method, which minimizes the probability of word errors [1]. A new class of convolutional codes called *turbo codes* was introduced by Berrou, Glavieux, and Thitimajashima [2]. It is well known for its extremely superior decoding accuracy. Hence, it has been widely adopted in modern wireless communication systems. The turbo decoder consists of two *soft-in-soft-output* (SISO) component decoders and operates by iterative decoding property. The soft-output algorithm described in the original turbo code paper [2] is usually known as the *maximum a-posteriori probability algorithm* (MAP) [3]. There are also many new researches about component decoders, such as *Soft-Output Viterbi-Algorithm* (SOVA) [4], Max-Log-MAP or Log-MAP algorithm [5].In general, the Log-MAP algorithm, which has better *bit error rate* (BER) performance than the SOVA and the Max-Log-MAP algorithm, is adopted to decode the data from the turbo encoder.

In the current 3G mobile wireless communication system standards [6][7], the voice and data streams are encoded by different types of FEC coding schemes, *i.e.* convolutional code and turbo code. Traditionally, the corresponding encoder/decoder schemes of convolutional and turbo codes are built in separate module and operated exclusively. To satisfy the advanced FEC standard, a VLSI design of a triple-mode VA/MAP *intelligent property* (IP) is proposed in Figure 1. We propose a *triple-mode timing chart* that can run VA and MAP concurrently by complementing the idle time of each other at the same time. Moreover, a reconfigurable FEC architecture based on *timing association* is also proposed to perform the FEC functions with high hardware efficiency. Thus, our design performs both VA and MAP functions at the same time. The chip area is only a little larger than the original turbo decoder, but it provides higher decoding throughputs.

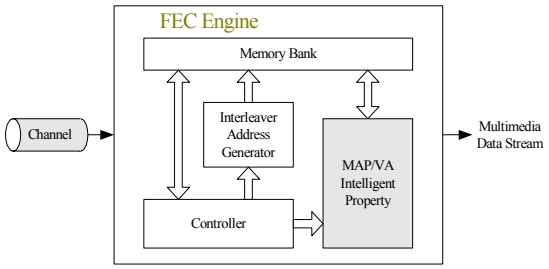

Figure 1. The proposed unified FEC engine.

II. TIMING ASSOCIATION

The concept of *timing association* is illustrated in Figure 2. The operations of both VA and MAP can be partitioned into two parts: the similar operation ($OP_{1,V,M}$) and the unique operations ($OP_{2,V}$ and $OP_{2,M}$). We assume that the similar operations need to wait unique operations; therefore, the similar operations have idle time. Figure 2(a) shows that one function is running when the other function is idle. We find that the utilization is about 50%. In Figure 2(b), we can concurrently perform both VA and MAP operations by complementing the idle time of each other and the utilization is near 100%. Thus, we can simultaneously improve the throughput rate and reduce the system latency. In recent research works, most existing dual-mode works [8][9], adopted the timing association of Figure 2(a). They perform

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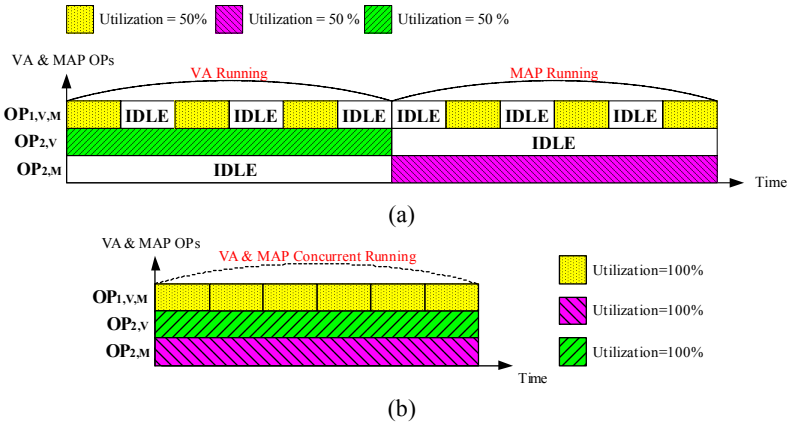

Figure 2. Timing association: (a) Exclusive operations, (b) Concurrent operations.

the VA and MAP exclusively rather than concurrently. In our design, we propose the *triple-mode MAP/VA timing chart* by complementing the idle time of each other as shown in Figure 2(b). As a result, we can increase the throughput rate, enhance the hardware utilization, and reduce decoding latency.

III. TRIPLE-MODE MAP/VA TIMING CHART

Based on timing association of Figure 2(b), we propose the triple-mode MAP/VA timing chart that includes three modes: *exclusive VA mode*, *exclusive MAP mode*, and *concurrent MAP/VA mode*. The concurrent MAP/VA mode indicates that the MAP and VA decoding are operating at the same time.

In the triple-mode MAP/VA timing chart (shown in Figure 3), the x-axis and y-axis denote the computing time and the decoding symbols, respectively. L is the sliding widow length that approximates five times constraint length K. The triple-mode MAP/VA timing chart uses the full parallel *Recursive Unit* (RU) that has the same number of *Add-Compare-Select* (ACS) units as transition states. In advanced communication systems, the constrain lengths of VA decoding and MAP decoding are different. For example, in WCDMA [6] or CDMA2000 [7], the constrain-length of Convolutional codes is *9* (*256* transition states), and the one of Turbo codes is *4* (*8* transition states).

In the evaluation of hardware cost and utilization, we use just *8* ACS units to compose a RU. Then, the RU performs full parallel recursion for MAP decoding and partial parallel recursion for VA decoding. Thus, the MAP decoder can perform one transition of *8* states each clock cycle, and the VA decoder must spend *32* clock cycles to perform one transition of *256* states. Figure 3 illustrates the practical realization of triple-mode timing chart. We set the sliding window length of MAP, *L, to 32*. Thus, in each time duration L of *32* clock cycles, the MAP operation completes one sliding window, and VA operation completes one stage (*256* states) of trellis. Therefore, in Figure 3, the unit of y-axis in MAP part is L (*32* stages per *32* clock cycles), and the one in VA part is 1 (one stage per *32* clock cycles). Besides, we let the sliding window length of VA $L'=45$. Therefore, VA operation completes one sliding window every *1440* clock cycles (L' stages * L clock cycles).

Finally, the concurrent MAP/VA mode executes both parts of the timing chart as shown in Figure 3. The exclusive MAP mode executes the MAP part of the timing chart in Figure 3 and the throughput of MAP mode is the same as the MAP part of concurrent MAP/VA mode. On the other hand, we find that the timing chart of the exclusive VA mode can be connected without sharing the RUF, as shown in Figure 4 and the throughput of exclusive VA mode become twice the VA part of concurrent MAP/VA mode.

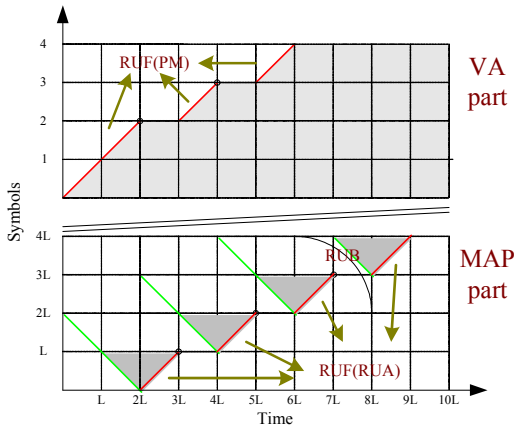

Figure 3. Timing chart of triple-mode decoding
(Convolutional codes with $K=9$ and Turbo codes with $K=4$).

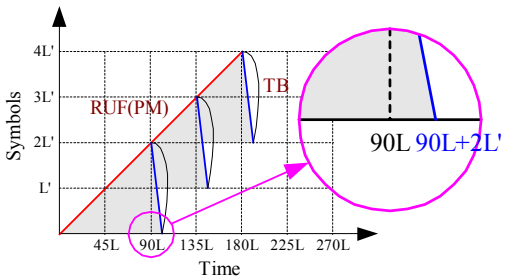

Figure 4. Timing chart of VA decoding.
(Zoom out horizontal axis)

IV. VLSI ARCHITECTURE DESIGN

To satisfy multiple advanced communication systems, a FEC engine (see Figure 1), is necessary to change some control signal or memory bank for different systems. Therefore, we propose a triple-mode MAP/VA IP, which can be reconfigured for different decoding methods and different parameters.

The datapath of the MAP/VA IP, including computing modules and memory blocks, is shown in Figure 5. The dotted areas are the storages. According to our proposed triple-mode MAP/VA timing chart, one RUF (PM/RUA) module, one RUB module, and one TB module are needed. Moreover, the distance between the received bits and each branch symbol is computed immediately for the RU, so the transition probability- computing units (BM/Gamma0 module and Gamma1 module) are built. Based on trellis decoding, the EETR0 module and EETR1 module can reconfigure trellis routers for different generator polynomial. The LLR module receives transition probability gamma values, forward recursive alpha values, and backward recursive beta values to obtain *LLR* values.

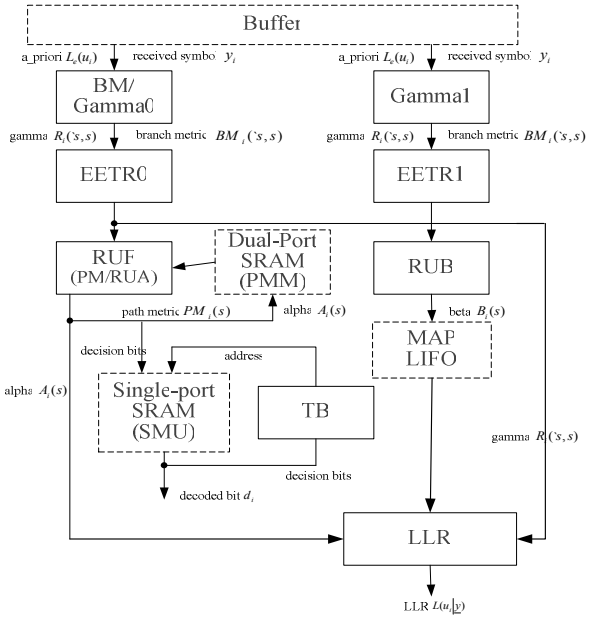

Figure 5. Architecture of the triple-mode MAP/VA IP

A. Exclusive VA Mode

According to the timing chart of VA mode in Figure 4, branch metrics $BM_i(S',S)$ are generated from the received symbol y_i. The BM/Gamma0 module computes the branch metrics $BM_i(S',S)$ and transmits into the RUF module to obtain path metrics $PM_i(S)$ via the EETR0 module. The RUF module includes *8* ACS units and obtains path metrics $PM_i(S)$ of *256* transition states in *32* clock cycles. In the procedure of recursion, we need the *2*8* dual-port SRAMs (PMM) to store *2*256* path metrics composed of old and updated values. *2* sliding window lengths (*2*45*) of decision bits are stored in the *Survivor Memory Unit* (SMU) block. Then, TB module can decode information by trace backing.

B. Exclusive MAP Mode

The IP uses two RUs that RUF module obtains forward recursive Alpha values $A_i(S)$ and RUB module obtains backward recursive Beta values $B_i(S)$. The transition probability-computing units (BM/Gamma0 module and Gamma1 module) obtain immediately the transition probability gamma values $R_i(S',S)$ used by RUs. The gamma values $R_i(S',S)$ are generated from the received symbol y_i. Then the gamma values $R_i(S',S)$ are transmitted to RU module via EETR module. We store Beta values $B_i(S)$ of each state at each time stage into MAP memory (LIFO block). The RUA module performs the Alpha operation and obtains Alpha values $A_i(S)$. At the same time, $L_i(u_i|\underline{y})$ is generated in the LLR module by the Alpha values $A_i(S)$, gamma values $R_i(S',S)$, and Beta values $B_i(S)$ fetched from LIFO block.

C. Concurrent MAP/VA Mode

According to the timing chart of Figure 3, the concurrent MAP/VA mode shares the BM/Gamma0 module, EETR0 module, RUF module. In the VA part, the BM/Gamma0 module performs the BM operation to obtain branch metrics $BM_i(S',S)$. Then, the RUF module performs the PM operation that fetches branch metrics $BM_i(S',S)$ via the EETR0 module, and obtains path metrics $PM_i(S)$. The TB module performs trace backing to obtain information bits. The decision bits d_i are generated in the SUM block. In the MAP part, the BM/Gamma0 module and the Gamma1 module perform the Gamma operations that fetches the received symbol y_i and extrinsic information $L_e(u_i)$ to obtain gamma values $R_i(S',S)$. Then, the RUB module performs the Beta operation that fetches gamma values $R_i(S',S)$ via the EETR0 module and generates Beta values $B_i(S)$, which are stored in MAP memory (LIFO block). The RUA module obtains Alpha values $A_i(S)$. At the same time, the LLR module uses the Alpha values $A_i(S)$, gamma values $R_i(S',S)$, and the Beta values $B_i(S)$ fetched from LIFO block, to generate *LLR* values $L_i(u_i|\underline{y})$.

D. Encoder Embedded Trellis Router (EETR)

For different transmission applications, data are encoded in different generating parameters. Therefore, it requires reconfigurable trellis architecture for each specification. We propose a method to reconfigure trellis architecture by using an encoder embedded counter. Based on trellis decoding, the encoder embedded trellis routers (EETR0 and EETR1) can be reconfigured for different generation parameters and code rates.

V. IMPLEMENTATION RESULTS

To illustrate our proposed techniques, we have implemented the triple-mode MAP/VA IP in an ASIC chip. At first, the design is realized using Matlab-to-RTL flow. In order to respond quickly to multiple advanced wireless communication systems, the Matlab and RTL codes of this

IP are generic and parameterized. The parameters include generator polynomials, interleavers for turbo codes, number of stages, control information, and overall finite word-lengths of the IP. The impact of each parameter affects the quality in terms of BER. To simplify BER simulation, a bit-true Matlab simulation model is created and the RTL model is realized with parameters extracted by Matlab model. Both models are functionally equivalent and verifiable. Figure 6 shows the finite precision performance of the triple-mode MAP/VA IP satisfying WCDMA standard with block size equaling to 1024.

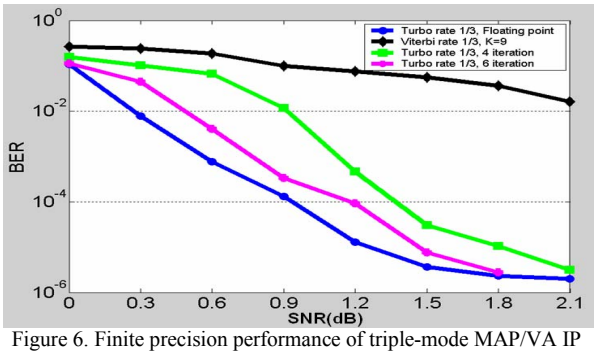

Figure 6. Finite precision performance of triple-mode MAP/VA IP

Figure 7 shows the layout of the chip using the TSMC 0.18 µm CMOS process with a die size 2.86 mm x 2.86 mm. We summarize the characteristics of the chip in Table I. For WCDMA standard, this IP can operate at clock frequency of 100 MHz and achieve throughput rate of (1) 3.12Mbps for Convolutional decoding in VA mode, (2) 4.17Mbps@6 iterations for Turbo decoding in MAP mode, and (3) 4.17Mbps@6 iterations for Turbo decoding and 1.56Mbps for Convolutional decoding in concurrent MAP/VA mode from the worst-case static timing analysis and post-layout simulation. We list the comparison in Table II and it shows that we can get better throughput rate. This IP is combined with external standard-dependent input/output buffers and interleaver logics for advanced wireless applications such as WCDMA or cdma2000 standards.

VI. CONCLUSIONS

In this paper, we investigated the timing association for combining VA and MAP in order to propose the triple-mode MAP/VA timing chart. Then, we proposed a triple-mode MAP/VA IP by sharing the similar components between MAP and VA. Thus, the proposed IP can be integrated into a FEC decoder with extra memory or interleaver logics for different applications: (1) Convolutional decoder, (2) Turbo decoder, (3) Dual-mode decoder, and (4) Triple-mode decoder. The design has been implemented in a 0.18µm CMOS process and this IP achieves better throughput rates than recent multi-mode FEC works.

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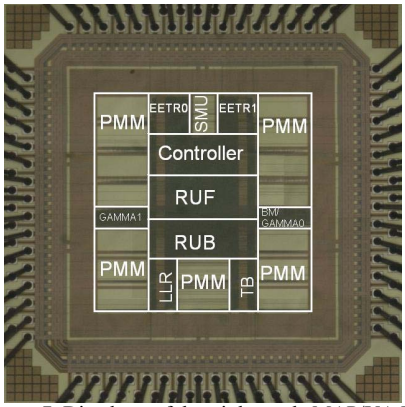

Figure 7. Die photo of the triple-mode MAP/VA IP.

TABLE I. CHIP SUMMARY OF THE TRIPLE-MODE MAP/VA IP.

Technology	TSMC 0.18um
Logic Gate	57.7K
Supply Voltage	1.8V
MAX. Frequency	100MHz
Power	320mW@100MHz
Die Size	2.86 x 2.86mm^2

TABLE II. COMPARISON OF THE SIMILAR FEC DECODER

		[9]	[8]	Proposed
Mode		Dual	Dual	Triple
Number of RU		1	2	2
Logic Gate Counts		46K	85K	57.7K
Max. Clock Frequency (Hz)		70M	128.8M	100M
Through-put (bps)	**Exclusive VA**	384K	1.54M	3.12M
	Exclusive MAP (6 it.)	12.2K	4.1M	4.17M
	Concurrent VA/MAP (6 it.)	192K (VA) 6.1K (MAP)	0.77M (VA) 2.05M (MAP)	1.56M (VA) 4.17M (MAP)