A LOW COST PACKET DETECTOR IN OFDM-BASED ULTRA-WIDEBAND SYSTEMS

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Abstract

Multiband orthogonal frequency-division multiplexing (MB-OFDM) systems employ frequency-hopping technology to achieve the capabilities of multiple access and frequency diversity. However, they also complicate packet detector (PD) in terms of the requirement for the high hardware complexity. In this paper, we propose several low-cost design schemes for the PD, such as Walsh-Hadamard decomposition, buffered summation, and sign-bit-remaining methods. The estimated gate count of the resulting implemented PD is less than half that of existing solutions.

1. INTRODUCTION

Multiband orthogonal frequency-division multiplexing (MB-OFDM) technology (or so-called *time-frequency interleaved OFDM*) has recently been applied to *wireless personal area networks* [1][2]. This technique increases both the traffic capacity and the frequency diversity. Furthermore, MB-OFDM employs several types of *time-frequency code* (TFC) in the *preamble* part to easily identify the *packet* properties and frequency-hopping sequences. However, even though MB-OFDM can lever the successful experience of other OFDM systems, such as *wireless local area network* (WLAN) [3][4], there are still many differences between MB-OFDM and conventional OFDM systems. These differences are often the bottlenecks of system performance. As illustrated in the dashed box of Fig. 1, the potential bottlenecks of the receiver front-end are as follows:

1) **Feedback control to the radio frequency circuit.** Controlling the hopping of the *radio frequency* (RF) circuit requires a feedback path from baseband to RF. The building blocks of the *analog*/RF circuit and the front-end for the baseband are shown in Fig. 1. z^D and z^P denote the latencies of *analog-to-digital converter*

(ADC) and *packet detector* (PD). z^R and z^C are the processing delays of the *controller* and the RF circuit. The processing delay of the feedback loop results in an *iteration bound* [7] that limits the system operation speed and performance.

2) **Large hardware complexity.** The receiver should identify different TFCs by detecting the *preamble* symbols of received *packets*. Hence, the order of the hardware complexity is proportional to both the frequency diversity and the types of *preamble*. For example, there are 6 *preamble* types for 6 band-hopping sequences, so the receiver PD has to handle 6 different cases and also has to control the RF hopping process very rapidly. In addition, because the OFDM symbols are transmitted sequentially in 3 bands [1], the channel parameters, such as the channel *group delays*, *channel impulse responses* (CIRs), and *carrier frequency offsets* (CFOs), are all unfolded 3 times. Huge hardware complexity is therefore unavoidable.

3) **Low power requirement.** MB-OFDM systems are often applied in portable devices, and hence low power consumption is also required.

Fig. 1 Critical components of the MB-OFDM receiver.

In this paper we systematically analyze the challenges and implementation difficulties of the MB-OFDM system, focusing on the baseband front-end circuits shown in the dashed box of Fig. 1. To address the above-mentioned difficulties, we propose a combined solution that

includes both performance and hardware improvements. The proposed methods are the *sign-bit-remaining method*, *Walsh-Hadamard (W-H) decomposition method*, *buffered-summation method*, and *pseudo noncausal relaxation (PNCR) method*.

2. HARDWARE IMPLEMENTATION PROBLEMS

In addition to the above issues, there are many stringent hardware implementation problems associated with MB-OFDM:

1) **Large hardware complexity for different TFCs:** To meet the spectrum mask of the RF band defined by the FCC, the MB-OFDM specification exploits coefficients of *preamble* sequences with more than 5-bit precision [1]. Moreover, there are 6 TFCs, each with 128 different taps. Therefore, if we implement the circuit directly (we denote the circuit as “*direct implementation*” in this paper), the total coefficients of the *matched filter* comprise $5 \times 128 \times 6$ bits. Low-cost design must therefore be considered both in the transmitter and the receiver.

2) **The RF-baseband iteration bound:** The building blocks of the RF and *baseband* circuits are shown in Fig. 1. Because *zero padding* is exploited in MB-OFDM to reduce the power consumption and the passband ripple [1], the receiver should postpone T samples to collect the *postcursor* of the OFDM symbol in order to add it back to the *overlap and add* (OLA) circuit. The circuit is denoted as the *overlap and add* (OLA) circuit. The total aforementioned delay should be less than the zero-padding length (denoted as ZP) between adjacent symbols, yielding

$$ZP \geq D + P + T + R + C. \quad (1)$$

Typical values used in the above equation are $ZP=37$, $D=5$ (pipeline ADC), $R=1$, $C=5$ (corresponding to a 9-ns switching time as proposed in [1] with a 1.89-ns sampling rate), and $P=4$ (by the unfolding 4 method [7]). Thus, the OLA delay T is less than 22, which is not met by the required OLA period T of channels *CM3* and *CM4* [4]. Therefore, the long latency of the feedback loop could degrade the performance for long-duration channels.

In Section 3 we derive our PD algorithm that can alleviate the above problems.

3 THE PD ALGORITHM

The proposed PD comprises the two major components shown in Fig. 2: the *Matched Filter* and *Power Meter*. In this section we briefly

introduce the algorithms for both components and the overall properties.

Fig. 2 Datapath block diagrams of the PD.

The proposed PD structure is shown in Fig. 2. The upper block in the figure is the matched filter, which is an *FIR* filter with *preamble* coefficients as filter coefficients, and the lower block is the *power meter*, which provides the power sum of tap data. Before deriving the algorithm, we explain the basic properties of the *preamble* coefficients of the MB-OFDM system. We define the *coefficient vector* as

$$\mathbf{C} \equiv [c_0, c_1, \dots, c_{N-1}]^T, \quad (2)$$

where the c_i variables are the *preamble* coefficients. The inner product of the coefficient vector is normalized as [1]

$$\mathbf{C}^H \mathbf{C} = N. \quad (3)$$

Because zero-padding signaling is adopted in the MB-OFDM system, the transmitted OFDM symbol can be expressed as the following vector form:

$$\mathbf{s}(n) = [s(n), s(n+1), \dots, s(n+W-1)]^T, \quad (4)$$

$$s(n) = \begin{cases} c_{((n))_W}, & \text{if } ((n))_W < N \\ 0, & \text{otherwise} \end{cases} \quad (5)$$

where $((n))_W$ denotes the remainder of n divided by W . From the quasi-orthogonal properties of the *preamble* coefficients, the cross-correlation between the coefficient vector and transmitted symbol vector is

$$[\mathbf{C}^T, \mathbf{0}_L^T]^T \mathbf{s}(n) = \delta(\kappa) + \nu(\kappa) \cong \delta(\kappa) \quad (6)$$

and

$$\kappa \equiv ((n))_W, \quad (7)$$

where $\delta(\cdot)$ is the *delta function*, $\mathbf{0}_L$ is the zero vector with length L , and $\nu(\cdot)$ is the small sidelobe signal which can be neglected because $\|\delta(0)\|^2 \gg \|\nu(\kappa)\|^2$ for all κ .

To simplify the derivation, we assume that the CFO is small, so the received signal of the *preamble* part can be expressed in the following matrix form [5]:

$$\mathbf{X}(n) = \mathbf{S}(n)\mathbf{h} + \mathbf{n}(n), \quad (8)$$

$$\mathbf{X}(n) = [x(n), x(n+1), \dots, x(n+W-1)]^T, \quad (9)$$

$$\mathbf{h} = [h_0, h_1, h_2, \dots, h_{N_m-1}]^T, \quad (10)$$

$$\mathbf{S}(n) = [s(n), s(n-1), \dots, s(n-N_m+1)], \quad (11)$$

where $\{h_l\}$ denotes the normalized CIR, N_m is the channel duration, and $\mathbf{n}(n)$ is the identical independent distribution (i.i.d.) noise vector with power σ_n^2 . Substituting Eq. (6) into Eq. (8) and assuming that the received signal power is σ_s^2 yields that the matched-filter output divided by $N\sigma_s$ is the estimator of the normalized CIR:

$$\frac{1}{N\sigma_s} \mathbf{C}^H \mathbf{X}(n) = \hat{h}_k + \mathbf{C}^H \sum_{k=0}^{N-1} \mathbf{n}_k(n). \quad (12)$$

The output power A_n of the matched filter is

$$A_k = \mathbf{C}^H \mathbf{X}(n) \mathbf{X}^H(n) \mathbf{C}. \quad (13)$$

Substituting Eq. (12) into Eq. (13) and taking the expectation value yields

$$\begin{aligned} \tilde{A}_n &\equiv E[A_n] = \mathbf{C}^H E[\mathbf{X}(n) \mathbf{X}^H(n)] \mathbf{C} \\ &= N^2 \sigma_s^2 |\hat{h}_k|^2 + N \sigma_n^2 \end{aligned} \quad (14)$$

Therefore, the expectation value of the average sum output is

$$\tilde{E}_n \equiv E[E_n] = \sum_{k=0}^{N+N_m-1} \tilde{A}_k = N^2 \sigma_s^2 + N_m N \sigma_n^2, \quad (15)$$

where we use the property of the normalized channel, that is,

$$\sum_{k=0}^{N+N_m-1} |h_k|^2 = 1, \quad (16)$$

and N_m is averaged channel length. Next, the power-meter output B_n and its expectation value are

$$B_n = \mathbf{X}(n) \mathbf{X}^H(n), \quad (17)$$

and

$$\begin{aligned} \tilde{B}_n &\equiv E[B_n] = E[\mathbf{X}(n) \mathbf{X}^H(n)] \\ &= N \sigma_s^2 + N \sigma_n^2. \end{aligned} \quad (18)$$

If a signal is not received or the signal in the matched filter does not match the coefficient vector (i.e. $\sigma_s^2 = 0$), the expectation value of the filter output can be derived from Eq. (14) and (18) as

$$\tilde{D}_n \equiv E[D_n] = \frac{\tilde{E}_n}{\tilde{B}_n} = \frac{N_m N \sigma_s^2}{N \sigma_s^2 + N \sigma_n^2} = N_m. \quad (19)$$

Otherwise, if the PD receives a *preamble* signal with correct timing, the matched-filter output is

$$\tilde{D}_n = \frac{N^2 \sigma_s^2 + N N_m \sigma_n^2}{N(\sigma_s^2 + \sigma_n^2)} = \frac{N \sigma_s^2 + N_m \sigma_n^2}{\sigma_s^2 + \sigma_n^2}. \quad (20)$$

To provide an intuitive understanding, we consider two extreme cases. First, for very high SNR (i.e., $\sigma_s^2 \gg \sigma_n^2$) the PD output is bounded by

$$\tilde{D}_n \approx N. \quad (21)$$

Second, for very low SNR (i.e., $\sigma_s^2 \ll \sigma_n^2$) the PD output is

$$\tilde{D}_n \approx N \cdot \text{SNR} + N_m. \quad (22)$$

The PD output is connected to the decision circuit (i.e., the Controller), and we can set a threshold level η in the Controller. If the PD output D_n is larger than the level in the Controller, this means that a packet has arrived. The properties of the proposed PD are as follows:

1. From the extreme case of Eqs. (21) and (22), the output is bounded from N to N_m , so the threshold level is independent of the input power.
2. The division E/B in Eq.(20) and in Fig. 2 can be avoided simply by checking the following inequality:

$$E_n \geq B_n \cdot \eta, \quad (23)$$

where η is the threshold level in the controller.

Finally, We define two measures to evaluate the performance of the PD system: the maximal correctly receiving probability (MCRP), which is given by

$$\text{MCRP} \equiv \max_{\eta} \{P_{\text{Normal}}(\eta)\}, \quad (24)$$

and the threshold range (TR) for which more than 90% packets are correctly received, which is given by

$$\text{TR} \equiv \max\{\eta\} - \min\{\eta\} \text{ for } \{\eta | P_{\text{Normal}}(\eta) \geq 0.9\}. \quad (25)$$

In next section, we will use the two measurements to judge the performance lose for different kinds of implementation method.

4 HARDWARE IMPLEMENTATION OF THE PROPOSED PD

As mentioned in Section 1, the hardware complexity of the PDs is very high, and so a low-cost design is essential. We also propose a PNCr method for relaxing the iteration bound in Eq. (1). For clarity, we list our implementation schemes and their purposes in Table 1.

Method	Applied Component	Purpose
<i>Sign-bit remaining</i>	<i>Matched filter</i>	Low cost
<i>W-H decomposition</i>	<i>Matched filter</i>	Low cost
<i>Buffered summation</i>	<i>Power meter</i>	Low cost
<i>PNCr</i>	<i>PD</i>	Relaxation of iteration bound

Table 1 Implementation methods and their purposes.

4.1 Only the sign-bit remaining in preamble coefficients

The coefficients in the matched filter are longer than 5 bits to fully meet the precision of the original specification. This long word length will increase the complexity of both the transmitter and receiver. We reduce the word lengths (and hence the hardware requirements)

using a *canonical sign digit* on the transmitter side and a word-length-truncation method on the receiver side.

Assume that the ideal received signal is a vector C as defined in Eq. (2) and that the truncated coefficient vector of the matched filter is C_{trun} . Table 2 lists the matched-filter output of $C^T C_{trun}$ for different truncated word lengths of the *preamble* coefficients. For the full word length, the value of $C^T C_{trun}$ is N (128), as shown by Eq. (3). It is evident that if there is only one bit (the sign bit) for each coefficient, the orthogonality property still holds true and the loss at the matched-filter output is only 0.778 dB.

Coefficient Word Length (bits)	Full	4	3	2	1 (sign)
Minimal $C^T C_{trun}$ for all TFCs	128	125	123	117	107
Relative loss (dB)	0	0.103	0.173	0.390	0.778

Table 2 The minimal matched-filter output for all TFCs for different truncated word lengths of the *preamble* coefficients.

4.2 W-H decomposition and matched-filter retiming method

Because only the sign information of the *preamble* coefficients needs to be kept in the matched filter with slight degradation, we can decompose each coefficient into two W-H subsequences [6] as follows:

$$C_i = A_i \oplus B_i, i = 1 \sim 6, \quad (26)$$

where $\oplus$ denotes the W-H product, C_i is the coefficient vector for the 6 TFCs, and A_i and the B_i are factorized coefficients with 16 and 8 taps, respectively. After applying W-H decomposition, the total order of the matched filter is reduced from 128 to (16+8) (i.e., a W-H hardware reduction factor of 128/(16+8)).

The hardware circuit of the decomposed matched filter is shown in Fig. 3(a). We retiming the FIR matched filter into the data broadcasting type [7] for consistency with the operating speed of 528 MHz. In addition, we precalculate the 1's complement of the input signal to be used in each *processing unit* (PU) as shown in Fig. 3(b), where s_k is the k^{th} coefficient (only one bit) of A_i or B_i . To further reduce the hardware complexity and avoid having to use an adder in the 2's complement converter (for multiplying by -1), we map multiplier coefficients of +1 and -1 onto 0 and 1, respectively. The adder in a traditional two's complement converter (i.e., 2's complement is 1's complement *plus 1*) is combined with the

adder in branch summation as shown in Fig. 3(c), where we use the carrier-in of the adder as the function of "plus 1". Applying the retiming method requires only one adder in the PU and no multiplier.

Fig. 3 (a) Cascaded W-H matched filter. (b) Broadcast-type retiming FIR filter. (c) Basic building block in both W-H filters.

4.3 Buffered summation to reduce the squaring circuit

Fig. 2 shows the 128 squaring circuits that are utilized to calculate the input signal power. However, we use the *buffered-summation* method to reduce the hardware complexity in a real implementation, as shown in Fig. 4. When new data arrive, we add the new squared data into the accumulator and subtract the oldest squared data from the accumulator. This implementation requires only two squaring circuits and two adders (one adder for adding new data and the other for subtracting the oldest data).

Fig. 4 Low-cost scheme of the power meter.

4.4 PNCR method

To relax the RF-baseband iteration bound as shown in Eq. (1), we approximate the matched-filter output as follows:

$$y[n] = \sum_{i=0}^{N-1} c_i x_{n-i}^k \approx \sum_{i=N-Q}^{N-1} c_i x_{n-i}^k + \sum_{i=0}^{N-Q-1} c_i x_{n-i}^{k-1}, \quad (27)$$

where the Q is the relaxation factor and k is the *preamble* symbol index. The principle of operation is demonstrated in Fig. 5. Fig. 5(a) shows the output waveform of the received data and the original output of the matched filter. If a *preamble* sequence is received, the matched filter of the PD will not detect the *preamble* symbol until the full FFT window of length N is filled. In contrast, Fig. 5(b) shows here Q samples of the previous *preamble* symbol are utilized to replace those data that are not yet received, because the current *preamble* is almost

the same as the previous one if there is no noise or frequency offset, and thus the total latency is relaxed from N to $N-Q$. For the first *preamble* symbol, the sensitivity of matched filter will be degraded by $(N-Q)/N$ because we do not have previous *preamble* data in this case. However, the estimation bias can be corrected in the second *preamble* symbol by using the FHC state machine. Therefore, the PNCR method will only slightly degrade the PD performance. In addition, the PNCR can also enhance the *bit error rate* (BER) by enlarging the postcursor region and adding the samples in the region into the FFT window using the OLA circuit.

Fig. 5 The PD output for (a) a typical approach waveform and (b) the PNCR method.

4.5 Cost-performance comparison of the low-cost PD

The calculated hardware reductions of the above low-cost design methods are listed in Table 3(a), where N is the number of points in the FFT, F_D is the W-H hardware reduction ratio, N_C is the original word length of the *preamble* coefficients in the matched filter, F_T is the word-length-reduction ratio of the *preamble* coefficient, and N_X is the input data word length. We assume that the complexity of an adder depends on the input width, and that the complexity of the multiplier is the product of the word lengths of both inputs. Using real numerical values in Table 3(a) results in Table 3(b), where $F_D=128/(8+16)$, $F_T=5$, $N=128$, $N_X=5$, and $N_C=5$. This indicates that the final gate count of the combination circuit is only 2.28% that of the direct implementation. In addition,

the hardware complexity is only half that in [8], where the cost-down approach reduces the tap number by 4, which degrades the performance by 6 dB (i.e., $10 \log_4$ dB).

We have introduced several low-cost implementation methods to reduce the area and power requirements. To clarify the performance degradation for each low-cost method, we define PDs I–IV to enable a fair comparison of the performance. The used methods for PDs I–IV are listed in Table 4, in which the related MCRP and TR are also given. The table indicates that the TR is degraded by 8.1 (i.e., $18.2-10.1$) after the fixed-point implementation. In addition, there is almost no degradation for the W-H decomposition (PD III) relative to the fixed-point version (PD II). The TR is further decreased by 2.7 (i.e., $9.8-7.1$) after the implementation of the PNCR in PD IV. However, all of the PDs meet the stringent

specification of the MCRPs all being larger than 10^{-5} .

5 CONCLUSIONS

We have described the difficulties both in algorithm and hardware implementations. We propose a PD that requires only 2.28% of the

gates and 50% of the hardware complexity relative to the direct implementation method and other existing solutions described in [8]. Moreover, the PD can cope with a worst-case SNR with a PDER of less than 10^{-5} .

Component	Device	Direct Implementation	After Coefficient Truncation (Factor: F_T)	After W-H Decomposition (Ratio: F_D)	After Buffered Summation	Final Design
Matched Filter	Adder	$(N-1)N_X$	-	$(N/F_D-1)N_X$	-	$(N/F_D-1)N_X$
	Multiplier	$N_C N_X N$	$N_C N_X N / F_T$	0	-	0
Power Meter	Adder	$(N-1)N_X$	-	-	$2N_X$	$2N_X$
	Squarer	$N N_C^2$	-	-	$2N_C^2$	$2N_C^2$

(a)

Component	Device	Direct Implementation	After Coefficient Truncation (Factor: F_T)	After W-H Decomposition (Ratio: F_D)	After Buffered Summation	Final Design
Matched Filter	Adder	635	635	115	115	115
	Multiplier	3200	640	0	0	0
Power Meter	Adder	635	635	635	10	10
	Squarer	3200	3200	3200	50	50
Total gate / remaining area Percentage		7670 100%	5110 66.62%	3950 51.50%	175 2.28%	175 2.28%

“-”: No modification

(b)

Table 3 Comparison of hardware complexity: (a) mathematical derivation and (b) numerical values.

PD scheme name	Implementation methods			Performance	
	Fixed Point	All low-cost methods without PNCr	All low-cost methods with PNCr	MCRP	TR
PD I	-	-	-	$>10^{-5}$	18.2
PD II	✓	-	-	$>10^{-5}$	10.1
PD III	✓	✓	-	$>10^{-5}$	9.8
PD IV	✓	✓	✓	$>10^{-5}$	7.1

“✓”/“-” denote using/not using the method.

Table 4 PD hardware schemes and related implementation losses.

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