A 19-mode 8.29mm² 52-mW LDPC Decoder Chip for IEEE 802.16e System
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Abstract
This paper presents a LDPC decoder chip supporting all 19 modes in IEEE 802.16e system. An efficient design strategy is proposed to reduce 31.25% decoding latency, and enhance hardware utilization ratio from 50% to 75%. Besides, we propose an early termination scheme that can dynamically adjust the number of iterations. The multi-mode chip can be maximally measured at 83.3MHz with only 52mW power consumption. The core area is 4.45mm² and the die area is 8.29mm².

Keywords : LDPC, IEEE 802.16e, and early termination.

Introduction
Low-density parity-check (LDPC) codes, which are one kind of linear block codes, have the best error-correcting performance approaching the Shannon limit [1]. Thus, LDPC codes have widely adopted by most advanced wire-line and wireless communication systems, such as IEEE 802.3an, 802.11n, and 802.16e. Recently, there are many interesting research works on LDPC codes [2]-[4]. However, there still exist many challenges, such as high routing complexity, large chip area, high power consumption, and multi-mode design. Therefore, we focus on the design and implementation of the 19-mode LDPC decoder for IEEE 802.16e system as shown in Table I.

Table 1 : 19-mode LDPC codes in IEEE 802.16e system.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Codeword a (bits)</th>
<th>Information bits k (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>576</td>
<td>288</td>
</tr>
<tr>
<td>2</td>
<td>672</td>
<td>336</td>
</tr>
<tr>
<td>3</td>
<td>768</td>
<td>384</td>
</tr>
<tr>
<td>4</td>
<td>864</td>
<td>432</td>
</tr>
<tr>
<td>5</td>
<td>960</td>
<td>480</td>
</tr>
<tr>
<td>6</td>
<td>1056</td>
<td>528</td>
</tr>
<tr>
<td>7</td>
<td>1152</td>
<td>576</td>
</tr>
<tr>
<td>8</td>
<td>1248</td>
<td>624</td>
</tr>
<tr>
<td>9</td>
<td>1344</td>
<td>672</td>
</tr>
<tr>
<td>10</td>
<td>1440</td>
<td>720</td>
</tr>
</tbody>
</table>

In this paper, we propose five design techniques for LDPC codes in IEEE 802.16e system: 1) overlapped operations of computational units for increasing hardware utilization ratio, 2) early termination scheme and 3) distributed memory banks for low power, 4) reconfigurable architecture for multi-mode design, and 5) efficient checkerboard layout scheme for low routing complexity and small chip area. Using TSMC 0.13um CMOS technology, the core area of this 19-mode decoder chip is only 4.45mm² with die size of 8.29mm². It can be maximally measured at 83.3MHz with only 52mW power consumption.

Proposed Design Strategy
A. Overlapped Operations of BNUs and CNUs
Traditionally, it is difficult to perform the overlapped operations of bit node units (BNUs) and check node unit (CNUs) given any parity check matrix based on Quasi-Cyclic LDPC codes. According to the algorithm in [5], we can reorder the base matrix, instead of reordering overall parity check matrix. The location of 1s could be gathered in the neighborhood of the diagonal, and it is easier to overlap the operations of the BNUs and CNUs with Min-Sum Algorithm (MSA) [6]. By this approach, the idle time can be reduced by 66%, the hardware utilization ratio can be enhanced from 50% to 75%, and the reduced ratio of decoding latency is 31.25% with respect to non-overlapped method.

B. Early Termination Scheme
An early termination scheme is proposed to make the LDPC decoder design more efficient and flexible. It can dynamically adjust the number of iterations when facing communication channels with different SNR values. The scheme is to store the hard-decision values and compare the decoded results in two successive iterations. If the decoded bits of this iteration are the same as those of previous iteration, the decoder is informed to terminate the operations. Otherwise, this mechanism would check whether the predefined maximum number of iterations is met or not. Once the termination condition is satisfied, the following block of pattern can be passed into the decoder and decoded iteratively.

C. Distributed Memory Banks
To enhance the data access parallelism, the storage elements can be implemented by 100 memory banks, which consist of 24 single-port and 76 two-port register files, instead of a central main memory. By activating the necessary memory banks, the operating frequency for system specification can be lower compared with the central main memory mechanism. Moreover, based on the distributed memory scheme, the power consumption is reduced for the mobile application.

D. Reconfigurable Architecture
In order to perform different block sizes of LDPC codes, we propose the reconfigurable architecture for multi-mode design as illustrated in Fig. 1. Since we find out the relationship of 19 parity check matrices in IEEE 802.16e system, our reconfigurable design can be achieved by Address Generation Unit (AGU) without modifying any storage elements and computational units. According to the signals form Counter Unit (CU), it is easy for AGU to generate the necessary address for BNUs, CNUs, Output Buffer and Early Termination Unit (ETU) by Look-up Table.

E. Efficient Checkerboard Layout Scheme
For lower routing complexity, we propose an efficient checkerboard layout scheme to arrange 100 memory banks in a 10x10 2-D array. Compared with other types of arrangement, the method of the uniformly distributed memory banks is suitable for low-cost LDPC chip implementation. The benefits are enhancement of core utilization ratio and reduction of the chip area.
Experimental Results

In simulation, at SNR of 4.0 dB, the decoding latency for (2304, 1152) LDPC codes can be reduced by 45% when maximum iteration is 8. Fig. 2 shows that the performance of our proposed decoding strategy with early termination scheme is almost the same as that of MSA [6].

Our decoder design is implemented and fabricated in TSMC 0.13um 1.2-V 1P8M CMOS technology. Fig. 3 shows the die photo of the fabricated chip design. The number of total gate counts is 420K. The core size is only 2.11mmx2.11mm and the die size is 8.29 mm². The maximum operating frequency is measured at 83.3 MHz, and the average power consumption is measured 52mW for 19-mode LDPC decoder. When activates the early termination scheme, the flexible throughput can be varied from 30.3Mbps of 8 iterations to 111.1Mbps of 2 iterations by dynamic adjustment.

In order to reduce power consumption and still meet minimum throughput requirement (15Mbps) for IEEE 802.16e system, we can reduce the core supply voltage to 0.85V. As shown in Fig. 4, the corresponding maximum operating frequency and power consumption are 41.67MHz and 16mW, respectively. The comparisons of our decoder design and other works are summarized in Table II.

Conclusion

This paper presents an efficient IC design strategy for QC-LDPC codes in IEEE 802.16e system. Our LDPC decoder design features smaller chip area, higher hardware utilization, lower decoding latency, flexible decoding throughput, and lower power consumption.

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References