

# Cost-Effective Echo and NEXT Canceller Designs for 10GBASE-T Ethernet System

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**Abstract**—In this paper, new echo and NEXT cancellers are proposed for echo and NEXT cancellation in full-duplex digital transmission over 10GBASE-T system. The proposed cancellation schemes inherit the concept of the adaptive interpolated FIR (AIFIR)-based crosstalk canceller, where the long portion is modeled by an adaptive sparse FIR filter. Furthermore, we also employ the channel shortening technique to shorten the impulse response of crosstalk interference. Hence, the complexity of echo and NEXT cancellers can be greatly reduced. Simulations show that compared with the conventional architecture, although the performance is degraded by 1.5dB, it still meets the SNR requirement in 10GBASE-T system. The complexity reduction of the proposed echo and NEXT cancellation schemes in arithmetic is about 70% and 65% respectively. The saving of hardware complexity results in computationally efficient VLSI implementation of the echo and NEXT cancellers in 10GBASE-T system.

## I. INTRODUCTION

In this paper, we take 10GBASE-T Ethernet [1] as our target system. In order to achieve the low cost property of Ethernet, the goal of this paper is to lower the cost of 10GBase-T DSP baseband. However, in the 10GBase-T system, the data transmission is divided into four wire lines and all of the four wire pairs are full-duplex. The 10GBase-T transceiver must be capable of dealing with the interferences, such as echo, near-end crosstalk (NEXT), and far-end crosstalk (FEXT). Conventional echo cancellation scheme [2][3] is that the echo canceller is an adaptive FIR filter to produce an echo replica. The received signal subtracts the echo replica to eliminate the echo interference. The architecture of the NEXT canceller is similar to echo canceller except the transmitter is now replaced by another transmitter which incurs the NEXT interference. In order to produce the echo replica, the echo canceller impulse response must be adapted to the echo impulse response. Thus, the complexity and cost of echo canceller is proportional to the length of echo impulse response. However, in the 10GBASE-T environment, the echo impulse response is very long. Implementing the echo canceller requires the adaptive FIR with hundreds of taps. Therefore, the echo and NEXT cancellers, which are hundreds of taps, dominate the cost of 10GBase-T baseband DSP. In this paper, new echo and NEXT cancellers are proposed. We employ the channel shortening technique [6][7] to shorten the echo and NEXT responses, and use adaptive interpolated-FIR (AIFIR) architectures [5] to greatly reduce the hardware

complexity. From system simulation results and cost-analysis, although the performance of the proposed transceiver architecture is degraded compared with the conventional, it can still meet the specification of 10GBase-T system. Moreover, compared with the conventional architecture, the cost saving of the proposed echo and NEXT cancellation schemes in arithmetic is about 70% and 65% respectively.

## II. REVIEW OF EXISTING COST-REDUCTION WORKS

### A. Adaptive Interpolated FIR Filter

One of the most computationally efficient implementations for narrow-band finite impulse response (FIR) filters is the interpolated FIR (IFIR) structure [4]. Fig. 1 shows the block diagram of an IFIR filter. The IFIR filter  $H(z)$  is given by

$$H(z) = F(z^L)G(z), \quad (1)$$

where  $L$  is the interpolation factor.  $F(z^L)$  and  $G(z)$  are described by:

$$F(z^L) = \sum_{k=0}^{N_F-1} f_{kL} z^{-kL}, \quad G(z) = \sum_{i=0}^{N_G-1} g_i z^{-i}. \quad (2)$$

where  $N_F$  is the number of the nonzero taps of the filter  $F(z^L)$ , and  $N_G$  is the length of the filter  $G(z)$ . Here,  $F(z^L)$ , is called the shaping filter with only every  $L_{th}$  sample being nonzero. Because  $F(z^L)$  has a very sparse impulse response, the number of arithmetic operations can be reduced greatly. The second FIR filter,  $G(z)$ , is a short-length interpolator filter which generates the missing samples by interpolation. Therefore, instead of generating all samples independently, we can design a decimated version of the filter, followed by an interpolator to generate other samples by interpolating between the existing samples. Typically, an IFIR filter requires approximately  $1/L_{th}$  of the multipliers and adders of a conventional equivalent FIR filter [8].

A typical echo response, shown in Fig. 2, consists of a short duration main section with wide variations followed by a long duration tail section similar to a slowly decaying exponential. In order to reduce the computational complexity of the echo canceller, a two-stage echo canceller was proposed in [5] as shown in Fig. 3. The first stage is the main echo canceller (MEC) that is used to cancel the main section of the echo response while the second stage, tail echo canceller (TEC), is used to cancel the tail section of the echo response.

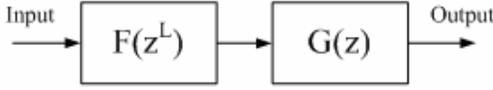


Fig. 1. Block diagram of Interpolated FIR

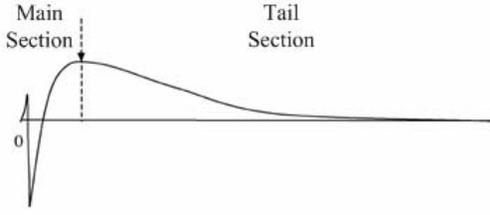


Fig. 2. Typical echo response

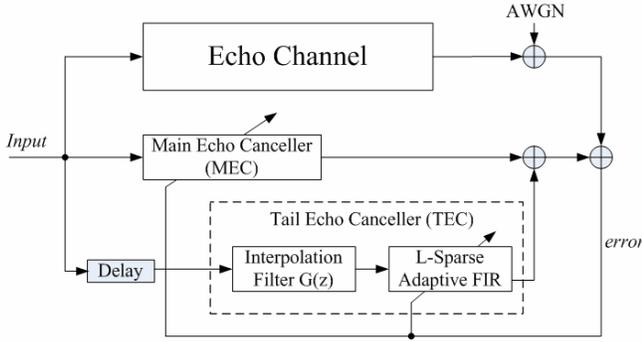


Fig. 3. The AIFIR-based echo canceller

Due to the general nature of main echo section, an adaptive direct-form FIR filter is employed in the MEC. However, because of the narrowband nature of tail echo section, an adaptive interpolated FIR (AIFIR) filter is employed in the TEC. The two-stage echo canceller has been shown to provide significant savings compared to the direct-form FIR echo canceller.

### B. Channel Shortening Technique

[6] reduces the cost of the echo canceller by employing the concept of channel shortening. In Fig. 4(a), a shortened impulse response filter (SIRF) is implemented at the echo path. The goal of SIRF is to shorten the echo impulse response to reduce the cost of echo canceller. Thus, the effective echo channel can be modeled as

$$h_{eff}(n) = h(n) * w(n). \quad (3)$$

Generally speaking, the length of the effective echo channel is greater than that of the original echo channel since the nature of the convolution operation. However, if we constrain most of the energy of the effective echo channel in consecutive  $\nu$  taps and assume  $\nu$  is smaller than the length of original channel, the channel shortening is achieved as shown in Fig. 4(b). Besides, because the largest  $\nu$  samples will not necessarily begin with the first samples, a delay parameter  $d$  is added to compensate at the receiver by delaying the start of the received symbols.

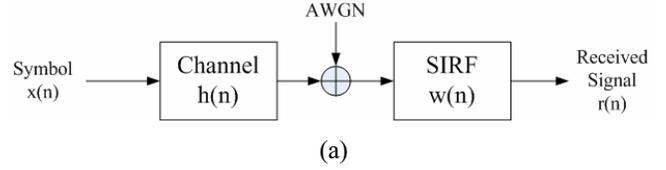


Fig. 4. Channel shortening concepts: (a) block diagram, (b) Impulses responses of original channel and shortened channel

From Fig. 4(b), if the original echo channel is shortened, the required tap length of echo canceller is reduced, and the cost of echo canceller can be reduced.

## III. PROPOSED COST-EFFECTIVE ECHO AND NEXT CANCELLATION SCHEMES

In this section, we propose a new echo cancellation scheme to greatly reduce the complexity of the echo canceller. The proposed scheme can also be applied to the NEXT canceller. Therefore, we can both reduce the cost of the echo and NEXT cancellers.

### A. Proposed Echo Cancellation Scheme

Fig. 5(a) shows the echo impulse response in 10GBASE-T system. We can find that the echo response is something different to the typical echo response in Fig. 2. The short duration main section with wide variations appears approximately in the middle region of the total echo response. Thus, the two-stage echo canceller [5] is not suitable to be applied in 10GBASE-T system. From Fig. 5(a), we can divide the echo response into three sections. Two long durations, head and tail sections, are similar to a slowly decaying exponential. One short duration, main section, is rapidly changing. In this paper, a three-stage echo canceller is proposed. The first stage is the head echo canceller (HEC) that is used to simulate the head section. The second stage is the main echo canceller (MEC) that is used to simulate the main section. And the third stage, tail echo canceller (TEC), is used to simulate the tail section. Due to the general nature of the main echo section, an adaptive direct-form FIR is applied in the MEC. Nevertheless, the narrow-band nature of the head and tail sections, two AIFIR filters are employed in the HEC and TEC, respectively.

In order to further reduce the complexity of the three-stage echo canceller, we also apply the channel shortening technique to the echo response. Fig. 5(b) shows the shortened echo response. The length of the main section is shorter than that of the main section of the original echo response in Fig. 5(a). Thus, we can use a lower-order direct-form FIR filter in the MEC. Although the total length of the head and tail sections becomes greater, the hardware increment is negligible

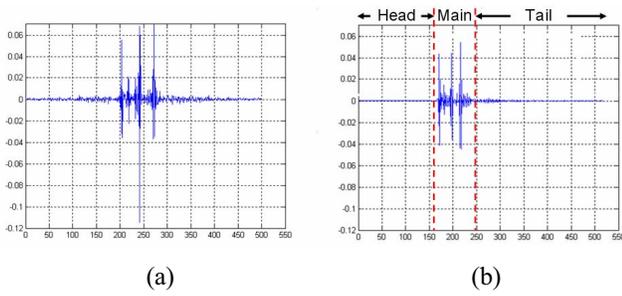


Fig. 5. Impulse response of echo (a) original, (b) shortened response with the Least Mean Square (LMS) approach.

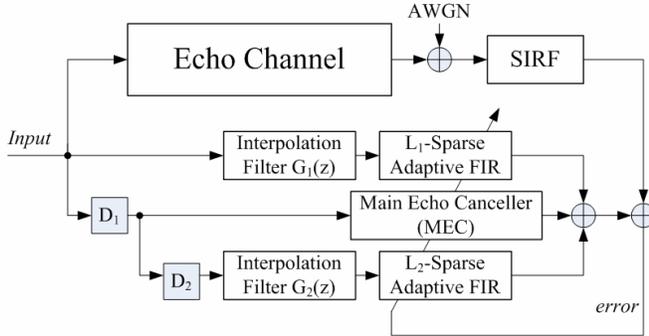


Fig. 6. Block diagram of the proposed echo canceller

owing to the fact that the AIFIR filters are applied in the HEC and TEC.

Finally, the proposed three-stage echo canceller architecture is shown in Fig. 6. A SIRF is used to shorten the echo response. The HEC, an AIFIR filter, consists of an interpolation filter  $G_1(z)$  and a  $L_1$ -sparse adaptive FIR filter, where  $L_1$  denotes the interpolation factor. The term,  $L_1$ -sparse, indicates that  $(L_1 - 1)$  null taps are inserted between every two successive taps. Besides, the TEC is another AIFIR filter consisting of an interpolation filter  $G_2(z)$  and a  $L_2$ -sparse adaptive FIR filter, where  $L_2$  denotes the interpolation factor. The term,  $L_2$ -sparse, indicates that  $(L_2 - 1)$  null taps are inserted between every two successive taps. The  $D_1$  delays can be used to align the MEC to accurately simulate the main section of the shortened echo response. Hence, the value of  $D_1$  equals to the length of the head section of the shortened echo response. Furthermore, the  $D_2$  delays can be used to align the TEC to accurately simulate the tail section of the shortened echo response. Hence, the value of  $D_2$  equals to the length of the main section of the shortened echo response.

### B. Proposed NEXT Cancellation Scheme

The shortened NEXT response is shown in Fig. 7. It is similar to the typical echo response in Fig. 2. We can model it with two parts, main and tail sections. Main section appears to be rapidly changing, while tail section appears to be relatively much smoother. Therefore, two-stage NEXT canceller is proposed here. The first stage is the main NEXT canceller (MNC) that is used to cancel the main section while the second stage, tail NEXT canceller (TNC), is used to cancel the tail section. In the MNC, an adaptive direct-form FIR filter is

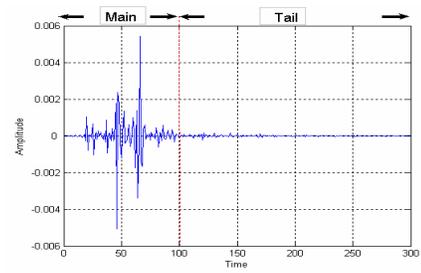


Fig. 7. The shortened impulse response of NEXT

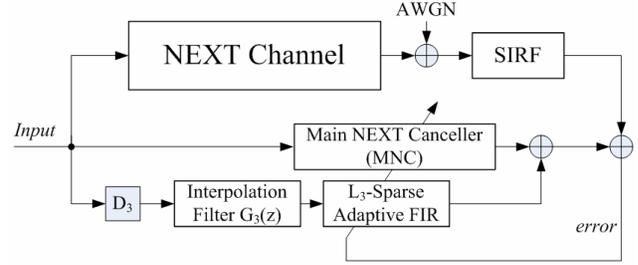


Fig. 8. Block diagram of the proposed NEXT canceller

applied. However, because of the narrowband nature of tail section, an adaptive interpolated FIR (AIFIR) filter is employed in the TNC.

Finally, the proposed two-stage NEXT canceller architecture is shown in Fig. 8. A SIRF is used to shorten the NEXT response. The TNC, an AIFIR filter, consists of an interpolation filter  $G_3(z)$  and a  $L_3$ -sparse adaptive FIR filter, where  $L_3$  denotes the interpolation factor. The term,  $L_3$ -sparse, indicates that  $(L_3 - 1)$  null taps are inserted between every two successive taps. The  $D_3$  delays can be used to align the TNC to accurately simulate the tail section of the shortened NEXT response. Hence, the value of  $D_3$  equals to the length of the main section of the shortened NEXT response.

## IV. PERFORMANCE ANALYSIS AND COST COMPARISON

In this section, we compare the conventional, [5], and the proposed architectures. The simulation results show that the complexity reduction of the proposed architecture is the greatest among these architectures.

### A. Floating-Point System Analysis

In the simulations, we apply the proposed echo and NEXT cancellation schemes to 10 Gigabit Ethernet applications. In 10GBASE-T systems, it achieves 10Gbps full-duplex transmission over 4 unshielded twisted pair (UTP) copper lines. The line coding is 16-level-pulse amplitude modulation (PAM16) over the UTP cat. 6. The cable length is 55m. Besides, in the channel equalization schemes, Tomlinson-Harashima Precoding (THP) is used to eliminate the post-cursor Intersymbol-Interference (ISI), while feedforward equalizer (FFE) is used to eliminate the pre-cursor ISI. The channel impairments that we consider here are the insertion loss, echo and NEXT available from IEEE 802.3an website [1]. We assume the receiver can operate in the correct sampling phase. The proposed transceiver architecture is shown in Fig. 9. For each line, we insert a SIRF at the receiver

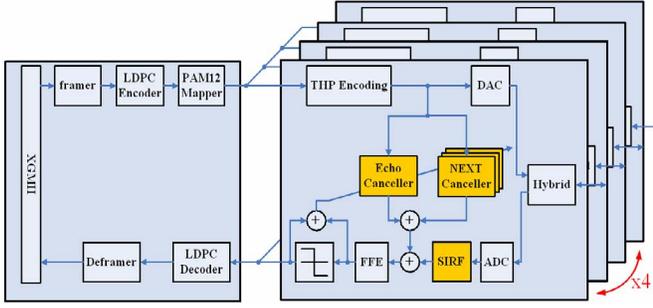


Fig. 9. The proposed transceiver architecture of 10GBASE-T system

to jointly shorten the echo and NEXT responses, and place the proposed echo and NEXT cancellers in the system. We add AWGN with 30dB SNR to model the interferences and noises other than echo and NEXT. The comparison of the equalizer output SNR with different structures is listed as the following Table I. We perform 200 randomly independent rounds and average the results. Compared the performance of the conventional with the proposed architecture, we have about 1.5dB loss in the output SNR. But the performance of the proposed architecture can still meet the SNR requirement, 23.4 dB, specified in 10GBASE-T.

### B. Implementation Cost Comparison

For an  $N$ -tap adaptive FIR filter with interpolation factor  $L$ , the required MACs are

$$\text{Arithmetic} = \frac{N}{L} + \frac{N}{L}. \quad (4)$$

In (4), the first term  $N/L$  represents the complexity of the filter, while the second term  $N/L$  represents the complexity of weight update.

Table II shows the complexity comparison of the echo cancellers, where  $L_1$  and  $L_2$  represent the interpolation factors. Compared with the conventional echo architecture in arithmetic, the cost saving of the proposed echo cancellation scheme and [5] is 69.80% and 59.60%, respectively. Besides, table III shows the complexity comparison of the NEXT cancellers, where  $L_3$  represents the interpolation factor. Compared with the conventional NEXT architecture in arithmetic, the cost saving of the proposed NEXT cancellation scheme and [5] is 64.83% and 44.17%, respectively. Therefore, among these architectures, our proposed echo and NEXT cancellers are the most cost-saving.

## V. CONCLUSION

In this paper, we propose low-complexity echo and NEXT cancellation schemes for 10GBase-T Ethernet system. We use a SIRF to shorten the echo and NEXT responses and combine AIFIR approach to greatly reduce the hardware complexity. Though the performance of the proposed transceiver architecture is degraded by 1.5dB compared with the conventional, but it still meets the specification in 10GBASE-T system. Moreover, the cost saving of the proposed echo canceller and NEXT canceller is about 70% and 65%, respectively.

TABLE I. EQUALIZER OUTPUT SNR OF DIFFERENT ARCHITECTURES

Architecture	Output SNR	Performance Gap
Conventional	26.33 dB	-
[5]	26.09 dB	0.24 dB
Our work	24.84 dB	1.49 dB

TABLE II. COMPLEXITY COMPARISON OF ECHO CANCELLER (EC)

Architecture	Conventional EC	[5]	Proposed EC
MEC	1000	150	120
$L_1$	-	8	8
HEC	-	40	40
$L_2$	-	4	8
TEC	-	160	40
Interpolator	-	54	62
SIRF	-	-	40
Total	1000	404	302
Saving	-	59.60 %	69.80 %

TABLE III. COMPLEXITY COMPARISON OF NEXT CANCELLER (NC)

Architecture	Conventional NC	[5]	Proposed NC
MNC	600	172	100
$L_3$	-	4	8
TNC	-	140	40
Interpolator	-	23	31
SIRF	-	-	40
Total	600	335	211
Saving	-	44.17 %	64.83 %

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