A 52-mW 8.29mm^2 19-mode LDPC Decoder Chip for Mobile WiMAX Applications

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Abstract - This paper presents a LDPC decoder chip supporting all 19 modes in Mobile WiMAX applications. An efficient IC design strategy is proposed to reduce 31.25% decoding latency, and enhance hardware utilization ratio from 50% to 75%. In addition, we propose a new early termination scheme that can dynamically adjust the iteration number. The multi-mode chip implemented in 8.29mm^{2}die area can be maximally measured at 83.3MHz with only 52mW power consumption.

Introduction

Low-density Parity-check codes, LDPC codes, have the best error-correcting performance approaching the Shannon limit [1]. Hence, LDPC codes have widely adopted by most modern wire-line and wireless communication systems, such as IEEE 802.3an, 802.11n, and 802.16e. Recently, there are many interesting research works on LDPC codes [2]-[5]. However, there still exist many design challenges, such as high routing complexity, large chip area, high power consumption, and multi-mode design. Therefore, we focus on the design and implementation of the 19-mode LDPC decoder for Mobile WiMAX applications as shown in Table I.

Table I : 19-mode LDPC codes in Mobile WiMAX applications.

Mode	Codeword n (bits)	Message k (bits)	Mode	Codeword n (bits)	Message k (bits)	Mode	Codeword n (bits)	Message k (bits)
1	576	288	8	1248	624	15	1920	960
2	672	336	9	1344	672	16	2016	1008
3	768	384	10	1440	720	17	2112	1056
4	864	432	11	1536	768	18	2208	1104
5	960	480	12	1632	816	19	2304	1152
6	1056	528	13	1728	864			
7	1152	576	14	1824	912			

In this paper, we propose five design techniques for LDPC codes in Mobile WiMAX applications: 1) overlapped operations of computational units for increasing hardware utilization ratio, 2) new early termination scheme and 3) distributed memory banks for low power dissipation, 4) reconfigurable architecture for multi-mode design, and 5) efficient checkerboard layout scheme for low routing complexity and small chip area. Using TSMC 0.13um CMOS technology, the core area of this 19-mode decoder chip is only 4.45mm^2 with die size of 8.29mm^2. It can be maximally measured at 83.3MHz with only 52mW power consumption.

Proposed Design Strategy

A. Overlapped Operations of BNUs and CNUs

Conventionally, it is difficult to perform the overlapped operations of bit node units, BNUs, and check node unit, CNUs, when given any Quasi-Cyclic parity check matrix. According to the algorithm in [6], we can only reorder the base matrix, instead of reordering whole parity check matrix. The location of 1s could be gathered in the neighborhood of the diagonal, and it is easier to overlap the operations of the BNUs and CNUs with Min-Sum Algorithm (MSA) [7]. Consequently, the hardware utilization ratio can be enhanced from 50% to 75%, and the reduced ratio of decoding latency is 31.25% with respect to non-overlapped method.

B. New Early Termination Scheme

A new early termination scheme is proposed to make the LDPC decoder design more efficient and flexible. It can dynamically adjust the iteration number for different communication channels with various SNR values. The scheme is to store the hard-decision values and compare the decoded results in two successive iterations. If the decoded bits of this iteration are the same as those of previous iteration, the decoder is informed to terminate the overall decoding operations. Otherwise, this mechanism would check whether the predefined maximum iteration number is met or not.

C. Distributed Memory Banks

To enhance the data access parallelism, the storage elements can be implemented by 100 memory banks, which consist of 24 single-port and 76 two-port register files, instead of a central main memory. By activating the needed memory banks, the operating frequency can be lower as compared with the central main memory mechanism. Moreover, based on the distributed memory scheme, the power consumption is reduced for the mobile wireless applications.

D. Reconfigurable Architecture

In order to support LDPC codes with 19 kinds of block sizes, we propose the reconfigurable architecture for multi-mode design as illustrated in Fig. 1. Our reconfigurable design can be achieved by Address Generation Unit (AGU) without modifying any storage elements and computational units. According to the signals from Counter Unit (CU), it is easy for AGU to generate the necessary address for BNUs, CNUs, Output Buffer, and Early Termination Unit (ETU).

E. Efficient Checkerboard Layout Scheme

For lower routing complexity, we propose an efficient checkerboard layout scheme to arrange 100 memory banks in a 10-by-10 2-D array. Compared with other types of placement, the method of the uniformly distributed memory banks is suitable for low-cost LDPC chip realization because of core utilization ratio enhancement and chip area reduction.

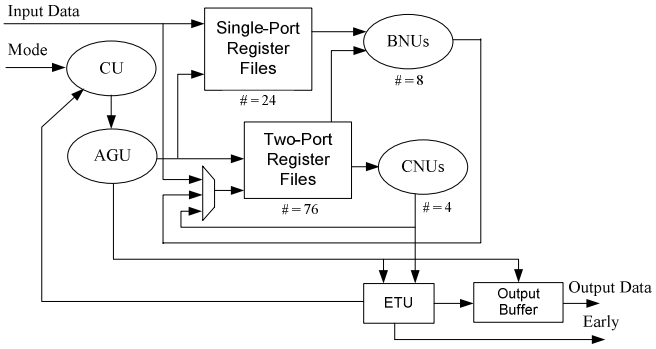

Fig. 1. Reconfigurable architecture of multi-mode design.

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Experimental Results

Fig. 2 shows the floating- and fixed-point simulation of (2304, 1152) and (576, 288) LDPC codes when the maximum iteration number is set to 8. The performance of our proposed decoding strategy with early termination scheme is almost the same as that of MSA [7] no matter what the block size is.

Fig. 3 shows the die photo of the multi-mode chip design, which is implemented and fabricated in TSMC 0.13um CMOS technology. The number of total gate counts is 420K. The core size is only 2.11mmx2.11mm, and the die size is 8.29 mm^2. The maximum operating frequency is measured at 83.3 MHz, and the average power consumption is measured 52mW for 19-mode LDPC decoder. By applying the early termination scheme, the flexible throughput can be varied from 30.3Mbps of 8 iterations to 111.1Mbps of 2 iterations by dynamic adjustment.

In order to reduce power dissipation and still meet minimum throughput requirement (15Mbps) for Mobile WiMAX applications, we can reduce the core supply voltage to 0.85V. As demonstrated in Fig. 4, the corresponding maximum operating frequency and power dissipation are 41.67MHz and 16mW, respectively. The comparisons of our decoder design and other works are summarized in Table II.

Conclusion

This paper presents an efficient IC design strategy for QC-LDPC codes in Mobile WiMAX applications. Our LDPC decoder design features smaller chip area, higher hardware utilization, lower decoding latency, flexible decoding throughput, and lower power consumption.

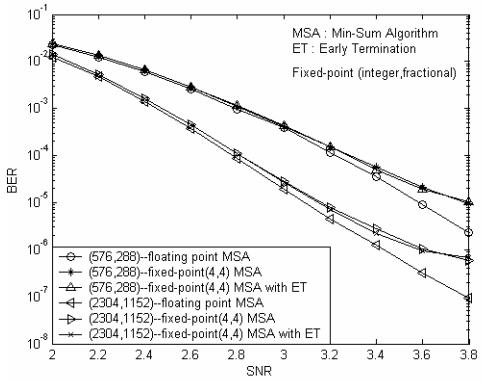

Fig. 2. Decoding performance comparison.

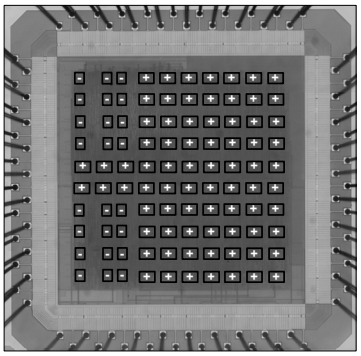

Fig. 3. Die photo. (- denotes single-port register files, and + denotes two-port register files)

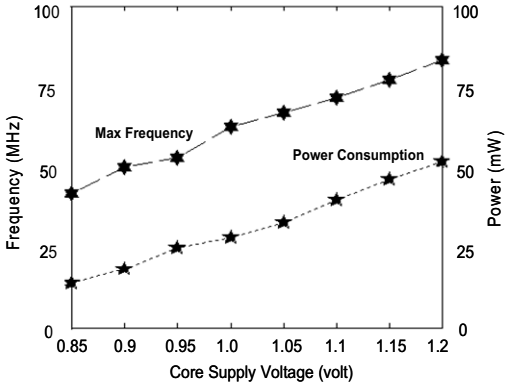

Fig. 4. Measured frequency and power consumption.

Table II : Chip comparison.

	JSSC'02 [2]	ISCAS'05 [3]	TCASI'06 [4]	JSSC'06 [5]	This work
Multi-mode	No	No	**No**	7 modes	**19 modes**
Spec	(1024,512)	(2048,1732)	**(1024,512)**	(2048,128*k) k = 8~14	**(96*k, 48*k) k = 6~24**
Code Construction	Random	RS-based	QC-based	Turbo-Interleaved	QC-based
Technology	0.16um	0.18um	0.18um	0.18um	0.13um
Parallelism	Fully	Fully	Partial	Partial	Partial
Iterations	64	32	8	16	2 ~ 8
Chip Area	52.5 mm^2	17.64 mm^2	10.08 mm^2	14.3 mm^2	8.29 mm^2
Frequency	64 MHz	100 MHz	200 MHz	125 MHz	83.3 MHz
Throughput	1 Gbps	3.2 Gbps	985 Mbps	640 Mbps	30~111 Mbps
Power	690 mW	N/A	N/A	787 mW	52 mW

Acknowledgement

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