POLAR TRANSMITTER FOR WIRELESS COMMUNICATION SYSTEMS

用於無線通訊系統之極座標發射機

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1. INTRODUCTION

Because of the demands of power efficiency and multi-mode of wireless mobile communication system increase, power efficiency is becoming more and more important in the device of mobile handset that can prolong the battery life. The problem concerning the critical power in mobile phone device is the RF power amplifier. We could increase the power efficiency by operating the power amplifier in the nonlinear mode. However, linearity is very important in avoidance of signal distortion which introduces spectrum growth, so we have to back off the input power of power amplifier in order to get more linearity. If we use the back off, power efficiency decreases.

Abstract

The transmitter architecture which we investigated is called polar transmitter. This architecture is different from conventional quadrature transmitter. Polar modulation techniques offer the capability of multimode wireless system and the potential for the high efficiency Power Amplifier (PA). As we know, any input signal of baseband message is decomposed into magnitude and phase signal, and then goes through envelope modulator and phase modulator respectively. The modulated envelope and phase message signals are combined and amplified by switched-mode PA. In this paper, we are going to focus on the rectangular-to-polar converter, envelope modulator and phase modulator of polar transmitter for EDGE (2.5G) system. The analog part includes open loop envelope modulator. The digital part includes rectangular-to-polar converter and digital phase modulator. We employ the Coordinate Rotation Digital Computer (CORDIC) and Direct Digital Frequency Synthesizer (DDFS) techniques in this part. A prototype chip has been designed and fabricated in UMC 0.18 μm CMOS process with 1P6M technology.

Keywords: polar, transmitter, DDFS, CORDIC.
In summary, either linearity or power efficiency must be traded off in the power amplifier. That is, we get more linearity while the power efficiency is decreased. Unless the modulation scheme is only phase modulated such as Gaussian Minimum Shift Keying (GMSK), a constant envelope modulation scheme, we could get higher power efficiency by operating the power amplifier into a nonlinear mode without backing off the input power level. However the number of information is increased recently, the data rate also has to be increased.

It is because the data rate has to be increased, the higher data rate is achieved by applying the non-constant envelope modulation scheme such as Enhanced Date rate for GSM Evolution (EDGE). According to that, linearity is a strict demand in the modulation scheme of non-constant envelope. Therefore, we have to search for the other transmitter architecture to meet the signal linearity and power efficiency at the same time.

Polar modulation offers the capability of achieving high linearity and high efficiency simultaneously in a wireless transmitter. Improved efficiency is achieved by using a highly efficient and non-linear PA to work at its peak efficiency. Linear transmission is achieved by modulating the envelope of the signal through the voltage supply of the PA.

Polar transmission utilizes envelope and phase component to represent the digital symbols instead of the conventional I/Q format [1]. The baseband signal $V(t)$ is split into the phase signal $\theta(t)$ and the envelope signal $A(t)$.

$$ V(t) = x(t) + j \cdot y(t), \quad (1) $$

$$ A(t) = \sqrt{x(t)^2 + y(t)^2}, \quad \theta(t) = \tan^{-1}\left(\frac{y(t)}{x(t)}\right). \quad (2) $$

It is clear that from Eq. (2) we can have a phase-only signal through phase modulator and multiplied with its envelope at the PA to recreate the original complex signal $\tilde{V}(t)$. This polar modulation process is like the Envelope Elimination and Restoration (EER) [2] architecture. In the conventional design, one part goes through a limiter to remove the envelope and keeps the phase information only. And the other part is detected by an envelope detector to extract the envelope information.

But both circuits would suffer from the non-linearity and distortion of the analog devices and would cause mismatch problem through the two paths. In this paper we proposed a DSP engine which includes rectangular-to-polar converter and digital Phase Modulator (PM). The design does not have the distortion problem caused by the analog components and the phase modulation process can be precisely controlled by the digital phase modulator. The baseband phase signal is modulated through digital phase modulator at the specific frequency range. The phase modulated signal is represented as $S_{IF-PM}(t)$.

$$ S_{IF-PM}(t) = \cos(w_c t + \phi(t)) \quad (3) $$

The PA stage of amplitude modulator (AM) operates in principle as a multiplier in our design model. This gives the output signal in the specific frequency band as follows:

$$ S_{IF}(t) = A(t) \cdot S_{IF-PM}(t), $$

$$ = A(t) \cdot \Re\{e^{j\phi(t)} \cdot e^{j\omega_c t}\}, $$

$$ = x(t) \cos(w_c t) + j \cdot y(t) \sin(w_c t). \quad (4) $$

For convenience of the simulation model [2], the gain of the PA is set to one. Thus the Eq. (4) is equal to the signal of EDGE, which is up-converted at Intermediated Frequency (IF) band. The non-linearity of PA and analysis of up-converter to Radio Frequency (RF) stage are beyond the scope of this paper.

### 2. POLAR TRANSMITTER ARCHITECTURE

The architecture of the polar transmitter is shown in Fig. 1. The rectangular-to-polar converter extracts the symbol phase and envelope information in the digital domain. Then the phase information is modulated through digital phase modulator to create a constant envelope and phase modulated signal. The phase modulated precision and channel selection can be well controlled in the digital part first. In this paper we use the concept from [3] to realize the digital phase modulator design. The digital fine-tune frequencies are generated by the DDFS. The DDFS interpolates...
the carrier frequencies between the coarse frequencies generated by the integer-N PLL. The main design considerations of the DSP engine include: (a) the bandwidth of the envelope and the phase signal; (b) the numbers of the fine-tune frequencies generated by the DDFS would affect the clock rate of DDFS and rectangular-to-polar converter; (c) the quantization effect in digital domain will cause phase noise and frequency spurs. And this effect also influences the Error Vector Magnitude (EVM) performance and the signal spectrum. Typically the bandwidths of envelope and phase signal are equal to 1 ~ 2 MHz and larger than the EDGE signal bandwidth 200 kHz. The clock rate of the DDFS can be derived [3] as below:

\[
f_{\text{clk}} = S \cdot f_{\text{sym}} > \frac{1}{0.4} \left( f_{\text{cs}} \times (N + 1) + \frac{f_{\text{fb}}}{2} \right)
\]

(5)

Where \( f_{\text{cs}} \) is the clock rate of DDFS, \( S \) is the number of samples per symbol and \( f_{\text{sym}} \) is the symbol rate of the EDGE signal. The maximum output frequency of DDFS is limited to 0.4 times the clock frequency. The parameter \( f_{\text{cs}} \) is the carrier spacing (200 kHz) in EDGE system, \( N \) is the number of digital fine tune frequency and \( f_{\text{fb}} \) is the transition BW of the filter which is located after up-converter stage. In our design, we choose \( N = 25 \), \( f_{\text{fb}} = 10 \) MHz, \( f_{\text{cs}} = 200 \) kHz and \( S = 96 \). Thus the clock rate of DDFS should be operated at 26 MHz. The digital fine tuning frequencies are generated by the DDFS and locating at 5 MHz ~ 10.4 MHz. Each interpolated frequency (channel) is stored in the fine-tune Frequency Control Word (FCW) table.

3. RECTANGULAR-TO-POLAR CONVERTER

For a coordinate axis converter, we adopt the CORDIC algorithm in our design since the CORDIC algorithm is very simple and low hardware cost. In order to further reduce the complexity, we also apply the technique in [4] to our rectangular-to-polar converter. For the first iteration we move the input vector into 1st and 4th quadrant with simply sign inversing and data exchanging. Second we replace \( y_i \) by \( y_i \cdot 2^{-i} \) as compared with conventional CORDIC algorithm. This modification can save once iteration and one barrier shifter in the rectangular-to-polar converter. This can save more area in our design. For \( i = 1 \) and input vector is \((x_1, y_1)\) from the EDGE signal:

\[
x_2 = d_i \cdot y_1, \quad y_2 = -d_i \cdot x_1, \quad z_2 = 0.5 \cdot d_i,
\]

\[
d_i = \text{sign}(y_i) = \begin{cases} 
-1, & y_i < 0 \\
1, & y_i \geq 0 
\end{cases}
\]

(6)

And the remaining iterations (for \( i = 2 \sim n \)) are shown in Eq. (7).

\[
x_{i+1} = x_i + d_i \cdot 2^{-2(i-2)} \cdot y_i, \\
y_{i+1} = 2 \left[ y_i - d_i \cdot x_i \right], \\
z_{i+1} = z_i + d_i \cdot p_i, \\
p_i = \frac{1}{\pi} \tan^{-1} \left(2^{-i-2}\right), \\
K = \frac{1}{\sqrt{\sum_i 1 + 2^{-2(i-2)}}}.
\]

(7)

The desired phase is \( z_{i+1} \) and the desired envelope value is \( x_{i+1} \) multiplied by a constant scaling factor \( K \). Due to the iterative feature of CORDIC algorithm, the clock rate of this module is \( n \cdot f_{\text{cs}} \), and \( n \) is iteration number. It is hard for the module to operate at such high clock rate. A compromise is to use unfolded technique and the architecture is shown in Fig. 2.

4. DIGITAL PHASE MODULATOR

The DDFS architecture is shown in Fig. 3. The DDFS has three basic blocks: FCW table, phase

![Fig. 2 Architecture of rectangular-to-polar converter](image)

![Fig. 3 Architecture of DDFS](image)
and phase-to-amplitude converter. The FCW table stores the desired fine-tune frequency control words and can be derived from Eq. (8).

\[ f_c = \frac{\text{FCW} \cdot f_{\text{clk}}}{2^L}, \quad \forall \text{ FCW} < 2^{L-1} \] (8)

In our design we focus on the phase-to-amplitude converter design and propose an architecture which is based on Least Squared (LS) algorithm [5] and Merged-Multiply Accumulator (MAC) technique [6]. The input phase is first truncated by 3-bit according to the \( \pi/4 \) symmetry and the amplitude of the sine function can be express by the polynomial. The approximated polynomial is generated according to the LS algorithm. In this paper we compare the Spurious Free Dynamic Range (SFDR) performance with the other approximation algorithm such as Taylor and Chebyshev [9]. The comparison method is set the input phase from 0 to \( \pi/2 \). The phase word-length is 15-bit and amplitude output is 15-bit. From the simulation result in Fig. 4, we can easily see that the LS-based polynomial can achieve better performance than Taylor and Chebyshev approximation algorithm with less polynomial order. The less order of polynomial means that low hardware complexity can also be achieved.

In order to reduce the polynomial order we further divide the approximated region into eight segments. In each segment, the approximated polynomial \( p(X) \) can be represented as in Eq. (9).

\[ p(X) = c_2 \cdot X^2 + c_1 \cdot X + c_0 \]

\[ = \sum_{i=0}^{n_1} R_i \cdot 2^i + [c_1]_{n_2} \cdot [X]_{n_3} + \sum_{k=0}^{n_3-1} C_k \cdot 2^k \]

\[ = \text{MAC} \left( \left[ \text{rom}_1 \right]_{n_i} + \sum_{j=0}^{n_2/2} Q_j \cdot [X]_{n_3} \cdot 4^j + \left[ \text{rom}_2 \right]_{n_3} \right) \] (9)

\[ Q_j = -2c_{1,2j+1} + c_{1,2j} + c_{1,2j-1}, \]

\[ c_{1,j} = 0, \quad 1 \quad \text{and} \quad c_{1,1} = 0, \]

\([ \ ]_n \) denote the truncation with \( n \)-bit. (10)

Where \( c_1 \) represents the coefficient, and \( X \) is the phase of each divided region. In Eq. (9) we store the first term and third term in the look-up table. The size of \( \text{rom}_1 \) and \( \text{rom}_2 \) are 1,536 bits and 232 bits respectively. The operations in Eqs. (9), (10) now become one booth multiplication and two constant additions. These can be merged into a modified-MAC (Fig. 5).

First the binary phase \( X \) is inputted to the booth decoder circuit and the partial product term is generated in each row of MAC. The partial product terms are summed through Carry-Save-Adder (CSA) tree. As compared with the direct implementation of \( 2^m \) order polynomial, the CSA tree can prevent the carry ripple problem in the early stages, and the carry ripple only occurs at the final stage. Due to the EDGE spectral requirement we target the desired SFDR over 80 dBc. From Matlab simulation, we set the truncated accumulated phase word-length to \( W = 15 \) bits and amplitude word-length to \( P = 14 \) bits. These hardware parameters can achieve SFDR = 86 dBc. The other parameter is the word-length of the phase of the EDGE signal. This will also introduce phase noise and spurs in the output spectrum and we will discuss in section 6. The proposed DDFS circuit is simulated by the NANOSIM tool and compares with state of the art in Table 1. It is obvious that the proposed DDFS can achieve high SFDR performance. The power efficiency is also superior to the other designs.

![Fig. 4 SFDR comparison between LS, Taylor and Chebyshev](image)

![Fig. 5 Architecture of Modified-MAC](image)
Table 1  Comparison with the existing DDFS designs

<table>
<thead>
<tr>
<th></th>
<th>DDFS</th>
<th>CMOS tech.</th>
<th>SFDR</th>
<th>Latency</th>
<th>Power efficiency (mW/MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ours</td>
<td>0.18</td>
<td>86</td>
<td>5</td>
<td></td>
<td>0.15</td>
</tr>
<tr>
<td>Ref. [7]</td>
<td>0.18</td>
<td>84</td>
<td>–</td>
<td></td>
<td>0.22</td>
</tr>
<tr>
<td>Ref. [8]</td>
<td>0.25</td>
<td>90.3</td>
<td>13</td>
<td></td>
<td>0.66</td>
</tr>
<tr>
<td>Taylor Ref. [9]</td>
<td>0.35</td>
<td>82.5</td>
<td>9</td>
<td></td>
<td>0.26</td>
</tr>
<tr>
<td>Chebyshev Ref. [9]</td>
<td>0.35</td>
<td>73</td>
<td>7</td>
<td></td>
<td>0.35</td>
</tr>
<tr>
<td>Ref. [10]</td>
<td>0.35</td>
<td>80</td>
<td>2</td>
<td></td>
<td>0.44</td>
</tr>
</tbody>
</table>

5  ENVELOPE MODULATOR

Given the bandwidth of the input signal would be limited in the close loop architecture; we had to increase the bandwidth of the filter in the close loop path. The wider bandwidth of the filter will introduce more and more noise to decrease the performance. Another drawback of the close loop approach used for mobile handset is the cost. The simpler architecture and circuit implementation is suitable for mobile handset. Based on these reasons, we tried an open loop approach to design the architecture of envelope modulator shown in Fig. 6. The pre-distorter is needed in the open loop architecture that will be further discussed later. From the simulation, we could define the number of input bits. Beside the bandwidth and consideration of cost, the circuit integration is another big issue. The inductance of the switched-mode power supply is too large to set on chip. The integration problem may cause many design problems and cost issues. Another design issues we faced is that the speed of the switching of the power transistor. Based on above investigation, we decided to adopt the power supply named linear regulator shown in Fig. 7 [11,12] at the cost of larger power dissipation. The linear regulator could provide faster switching rate and no inductance is needed. Note that before the linear regulator, it has to add DAC to convert the digital signal to analog signal.

We selected BCP69 [13,14] as the power transistor called Q1.BCP69 that could supply with high current up to 1A and be linear voltage regulator in application. According to data sheet of Analog Device, we selected AD8036 as the comparator called OP1 in the preliminary design. AD8036 is an operation amplifier with low distortion, wide bandwidth voltage feedback clamp.

5.1 Nonlinear Effect of PA

The nonlinear model in the envelope modulator is very important to investigate the circuit performance. We just use nonlinear model to replace the PA because we didn’t design the PA in this work. We simply use more accuracy model of PA to represent PA is enough.

Memory effect is an important effect and critical issue in power amplifier. Memory effect not only affects the accurate of the model, but affects the operation of the linearization of circuit. But memory effect is too complex to analyze and measure. In this paper, we only knew the memory effect has a big influence on the design of polar transmitter. As for the investigation and measurement of memory effect, we will make our effort to finish it in the future.

Beside we could not get a more accurate and non-memoryless nonlinear model of PA, the AM-to-AM model of the power supply of PA to the output amplitude of PA isn’t available. Now, we just use Rapp model which is memoryless and AM-to-AM model of the input amplitude to output amplitude of PA. Although nonlinear models below aren’t suitable for the pre-distorter design of envelope modulator, we proved that nonlinear models could be linearize by predistortion.

The function of AM-to-AM and AM-to-PM model of Rapp model is listed in Eqs. (11), (12). Rapp model is proposed by C. Rapp in 1991 [15]. Rapp model described by (11), (12) models the nonlinear effect in 4DPSK/OFDM system. These two AM/AM and AM/PM models match with measurements of actual
class-AB mobile phone amplifier. Now many nonlinear problems of PA use this model in many communication systems. $V_{sat}$ and $c$ represent input saturation voltage and the maximum phase shift caused by PA. Figures 8(a) and 8(b) illustrate the model we use in the later simulation.

$$V_{out} = \frac{V_{in}}{1 + \left(\frac{V_{sat}}{V_{in}}\right)^2}^{1/(2P)}$$  \(11\)

$$\phi(r) = c \times \left(\frac{V_{in}}{V_{sat}}\right)^4$$  \(12\)

### 5.2 Predistortion

Figure 9 illustrates the predistortion. The principle theory of predistortion is to transfer the input signal to the nonlinear one before putting it into the power amplifier; after the input signal goes through the power amplifier of nonlinear predistortion, the output signal will be similar to the linear of transformation.

Because this work focuses on envelope modulator, we only make predistortion compensation for AM-to-AM nonlinear model. If we know the AM-to-PM model precisely, we could make predistortion compensation precisely or rotate the phase to get the right signal constellation. We don’t need to make effort on phase predistortion. Besides the reason, the measurement of AM-to-PM is difficult especially for modulated signals. In conclusion, getting the more precise AM-to-PM nonlinear model under the EDGE modulated signal is very difficult.

In this work, we adopted the polynomial curve fitting to fit the nonlinear curve and fit the inverse curve by numerous methods. At the first step, we get the input amplitude (volt) and output amplitude (volt) to make up the nonlinear curve to fit the nonlinear polynomial $P_{nonlinear}(v_{in})$. At the second step, we make the wanted linear curve of input amplitude to output amplitude $P_{linear}(v_{in})$, i.e., constant gain. At the third step, we solve the root of the polynomial $P_{nonlinear}(v_{in},\text{want}) = P_{linear}(v_{in})$. After solving the roots of the polynomial, we could get the inverse polynomial $P_{inverse}(v_{in})$.

For example, we use 9-th curve fitting

$$P_{nonlinear}(v_{in}) = \sum_{i=0}^{9} a_i \times v_{in}^i$$  \(13\)

$$P_{linear}(v_{in}) = Gain_{linear} \times v_{in}$$  \(14\)

Solving the roots of the equation

$$P_{nonlinear}(v_{in,\text{want}}) = P_{linear}(v_{in})$$  \(15\)

we could get the approximate root $v_{in,\text{want}}$, then we could obtain the inverse polynomial $P_{inverse}(v_{in})$.

Now, we use 9-th order polynomial curve fitting

$$P_{inverse}(v_{in}) = \sum_{i=0}^{9} b_i \times v_{in}^i = v_{in,\text{want}}$$  \(16\)

as

$$P_{nonlinear}(P_{inverse}(v_{in})) = P_{nonlinear}(v_{in,\text{want}}) = Gain_{linear} \times v_{in} = P_{linear}(v_{in})$$  \(17\)
As the above description, we can get the approximate nonlinear polynomial $P_{\text{nonlinear}}$ of Rapp model, the linear polynomial $P_{\text{linear}}$ and the inverse polynomial $P_{\text{inverse}}$ of approximate nonlinear polynomial $P_{\text{nonliner}}$. The respective curve is shown in Fig. 10.

6. SIMULATION RESULT

6.1 Phase Modulator

For Mobile Station (MS), the requirements of EVM-rms and EVM-peak are below 9% and 30%. For Base-Transceiver Station (BTS) EVM-rms and EVM-peak are below 7% and 22%. The SFDR performance of the digital frequency synthesizer is suitable for the up-link and down-link spectral requirement. But the phase signal word-length also contributes spurs and phase noise. And the wordlength also affects the EVM and the signal spectrum. In this paper we simulate the finite word-length ($J$) effect of the phase signal with the EVM measurement and spectral mask requirement. The performance summary is in Table 2.

From the Table 2, we can see that the errors produced by the phase quantization are very small for the word-length higher than 9-bits. And the errors introduced by the entire digital phase modulator can be eliminated. But the spectrum of the $s_{\text{IF,psd}}(t)$ signal is not exactly below the spectral mask. Especially for BTS-mask, the requirement of the mask is more stringent than MS-mask. Since the quantization phase error will degrade the synthesizer SFDR performance. It is conservative to choose $J = 12$-bit in our design. The signal spectrum with $J = 12$-bit at the carrier which equals to 8 MHz is shown in Fig. 11. The digital phase modulated signal generated by the DDFS can meet the spectral requirement for BTS-mask and MS-mask.

6.2 Envelope Modulator

The below simulation is based on the architecture of the polar transmitter in the ADS environment. We have shown some simulation results, power spectrum and EVM. These two simulation results show the performance of the polar transmitter system for EDGE in the condition of PA nonlinear model. Because of the nonlinearity, we adopted the pre-distortion method to linearize the PA.

6.2.1 Without pre-distortion

Figure 12 shows the simulation block of nonlinear model without predistorter. Note that the block diagram of DDFS and Up-converter is the phase modulator. The spectral performance which touches

Table 2 Simulation result and EVM measurement

<table>
<thead>
<tr>
<th>J-bits</th>
<th>EVM-rms</th>
<th>EVM-peak</th>
<th>Spectral requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>9-bits</td>
<td>0.028%</td>
<td>0.094%</td>
<td>No (Spurs at – 66 dBc)</td>
</tr>
<tr>
<td>10-bits</td>
<td>0.014%</td>
<td>0.046%</td>
<td>No (Spurs at – 74 dBc)</td>
</tr>
<tr>
<td>11-bits</td>
<td>0.007%</td>
<td>0.018%</td>
<td>No (Spurs at – 79 dBc)</td>
</tr>
<tr>
<td>12-bits</td>
<td>0.003%</td>
<td>0.011%</td>
<td>Yes (Spurs at – 81 dBc)</td>
</tr>
</tbody>
</table>
the spectral mask is shown in Fig. 13. The EVM performance is 8.5% near the 9% of EVM requirements.

6.2.2 With pre-distortion

Figure 14 shows the simulation block of nonlinear model with predistorter. The spectral performance which does not touch the spectral mask to meet the spec. is shown in Fig. 15. The EVM performance is 3.6% smaller than the 9% of EVM requirements.

6.3 Delay Skew of Polar Transmitter

Figure 16 shows the simulation block of polar transmitter with variable delay which is used to simulate the delay mismatch between the envelope and phase signal. In order to discuss the delay skew of polar transmitter only, we omit the nonlinear effect of PA such that predistorter is removed here.

The EVM performance (Fig. 17) with delay mismatch equals 120 ns is smaller than the 9% of EVM requirements. The spectral performance (Fig. 18) with delay mismatch equals meet the spectral mask. In summary, the maximum allowable delay mismatch between envelope and phase signal is 60 nsec.

7. IMPLEMENTATION RESULT

The proposed DSP engine was implemented in UMC 0.18 μm CMOS process with 1P6M technology. The layout of the DSP engine is shown in Fig. 19. The summary of the circuit is list in Table 3.

8. CONCLUSION

In this paper, we proposed the DSP engine for the polar transmitter. The engine is realized by the CORDIC and DDFS techniques. In the digital phase modulator we adopt the LS algorithm. We also apply MAC technique in our DDFS architecture to reduce the hardware complexity and decrease the carry ripple problem of the direct polynomial implementation.

The power supply of envelope modulator is the architecture of linear regulator because the integration of inductance in the SMPS architecture is very difficult. In this work, we hope that the polar transmitter is highly integrated in mobile handset, for the existence of inductance isn’t suitable. We adopted the linear regulator architecture rather than SMPS at the cost of larger power dissipation. The envelope modulator of the open loop architecture is adopted because it is suitable for mobile handset and wideband modulation scheme.
The chip implementation with UMC 0.18 μm CMOS process with 1P6M technology is also presented in this paper.

REFERENCES


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