Low-Power Memory-Reduced Traceback MAP Decoding for Double-Binary Convolutional Turbo Decoder

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Abstract—Iterative decoding of convolutional turbo code (CTC) has a large memory power consumption. To reduce the power consumption of the state metrics cache (SMC), low-power memory-reduced traceback maximum *a posteriori* algorithm (MAP) decoding is proposed. Instead of storing all state metrics, the traceback MAP decoding reduces the size of the SMC by accessing difference metrics. The proposed traceback computation requires no complicated reversion checker, path selection, and reversion flag cache. For double-binary (DB) MAP decoding, radix-2 $\times$ 2 and radix-4 traceback structures are introduced to provide a tradeoff between power consumption and operating frequency. These two traceback structures achieve an around 20% power reduction of the SMC, and around 7% power reduction of the DB MAP decoders. In addition, a high-throughput 12-mode WiMAX CTC decoder applying the proposed radix-2 $\times$ 2 traceback structure is implemented by using a 0.13- μ m CMOS process in a core area of 7.16 mm². Based on postlayout simulation results, the proposed decoder achieves a maximum throughput rate of 115.4 Mbps and an energy efficiency of 0.43 nJ/bit per iteration.

Index Terms—Low-power design, maximum *a posteriori* (MAP) algorithm, turbo decoder.

I. INTRODUCTION

SINGLE-BINARY (SB) convolutional turbo code (CTC), proposed in 1993 [1], has been proven to provide a high coding gain near the Shannon capacity limit. The SB-CTC has been adopted in the forward-error-control (FEC) scheme for wideband code-division multiple access (WCDMA) [2] and cdma2000 [3]. In 1999, the nonbinary CTC [4] was introduced, which has a superior coding performance compared with the SB CTC [5]. In recent years, double-binary (DB) CTC has been adopted in the FEC coding of advanced wireless communication standards, such as digital video broadcasting-return channel over satellite and terrestrial (DVB-RCS

Fig. 1. Decoding path of the state metrics access: the (a) conventional path and (b) traceback path.

and DVB-RCT) [6], and worldwide interoperability for microwave access (WiMAX) [7].

Powerful soft-input soft-output (SISO) algorithms for CTC decoding are the maximum *a posteriori* algorithm (MAP) [8], and its derivatives, such as the log-MAP (L-MAP) [9], Max-log-MAP (ML-MAP) [9], combinations of the L-MAP and ML-MAP [11], and enhanced Max-log-MAP (EML-MAP) [12]. In this paper, we use the term MAP for an abbreviation of L-MAP and (E)ML-MAP.

The memory organization of MAP decoding is an important issue in facilitating the hardware implementation of CTC decoders [13]. In particular, the power reduction of state metrics cache (SMC) is critical for MAP decoders [14]. With regard to SB CTC decoding, some researches have been proposed to reduce the power consumption of the SMC [14]–[21]. The reverse computations [20], [21] significantly reduce SMC power consumption with reversion checkers and reversion flag caches. However, the reversion checker and reversion flag cache prolong the critical path or decoding cycles. In addition, the computational complexities of the reverse computations are increased dramatically when the reverse computations are extended from the SB to the DB MAP. Although some researchers [22], [23] have proposed the VLSI designs of DB CTC decoders, there are presently very few papers discussing an efficient SMC power reduction of DB CTC decoders.

In this paper, the traceback MAP decoding is proposed to trace the state metrics back by accessing the difference metrics. Fig. 1 illustrates the decoding paths of the conventional computation and proposed traceback computation. In the conventional path, the state metrics computed by the natural recursion processor (NRP) in the natural order are stored in the SMC.

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Decisions $u_k = z$ are based on

$$z = \arg_z \left(\text{MAX} \left(\Lambda_{\text{apo},k}^{(00)}(u_k), \Lambda_{\text{apo},k}^{(01)}(u_k), \Lambda_{\text{apo},k}^{(10)}(u_k), \Lambda_{\text{apo},k}^{(11)}(u_k) \right) \right). \quad (2)$$

Note that the values of $\Lambda_{\text{apr},k}^{(00)}$, $\Lambda_{\text{apo},k}^{(00)}$, $\Lambda_{\text{ex},k}^{(00)}$, and $\Lambda_{\text{in},k}^{(00)}$ are always equal to zero.

The differences between the DB L-MAP and DB (E)ML-MAP are that *a priori* LLR multiplies the channel value, and MAX operations are replaced by MAX* in the DB L-MAP. The MAX* [9] is defined as

$$\text{MAX}^*(x, y) = \ln(e^x + e^y) = \text{MAX}(x, y) + \ln(1 + e^{-|x-y|}). \quad (3)$$

A lookup table (LUT) can implement the corrective term $\ln(1 + e^{-|x-y|})$. The difference between the DB EML-MAP and DB ML-MAP is that the extrinsic values in the DB ML-MAP do not multiply a scaling factor.

Despite the SB and DB MAP decoding, the L-MAP has the significant coding gain and the EML-MAP achieves better coding gain than the ML-MAP. Without specifying which algorithm is used, we use the term MAP for an abbreviation of the L-MAP and (E)ML-MAP in the following sections. The details of SB MAP algorithms can be referred to in [10] for the SB CTC.

III. POWER REDUCTIONS OF STATE METRICS CACHE

Before we introduce the proposed memory-reduced traceback MAP decoding, the background information of SMC power reduction for the MAP decoding is demonstrated in this section.

A. Conventional (Windowing) Decoding Procedure

Despite the SB or DB MAP decoding, 2^{v-1} forward (1b) and 2^{v-1} backward (1c) recursion states metrics are computed in chronologically reverse order, where v is the constraint length of a RSC encoder. Both forward and backward recursion state metrics are required for the computation of *a posteriori* LLR (1d). Thus, a large SMC stores the forward (or backward) recursion state metrics to compute the *a posteriori* LLR until the backward (or forward) recursion state metrics are generated. The conventional decoding procedure employing the windowing technique [25] was proposed to reduce the depth of SMC from a block size (N) to a window size (L), where L is $4v \sim 6v$. (The well-known sliding window (SW) and parallel window (PW) MAP architectures can be referred to in [13] and [26], respectively.) Fig. 3 shows the conventional decoding procedure. In the natural order, the NRP, composed of 2^{v-1} add-compare-select units (ACSU), is used to recursively compute the $L \times 2^{v-1}$ forward (or backward) recursion state metrics in L cycles. The obtained 2^{v-1} state metrics in each cycle are immediately stored into the SMC and recursively fed back to the NRP to calculate the next 2^{v-1} state metrics. To compute the *a posteriori* LLR, the 2^{v-1} state metrics are read out from the SMC. The SMC of the conventional decoding procedure still accounts for more than 50% of the entire power consumption [14].

Fig. 3. Conventional decoding procedure.

Fig. 4. Reverse decoding procedure.

B. Reverse Decoding Procedure

To further reduce the access power of SMC, the reverse computations [20], [21] modified the conventional decoding procedure for the radix-2 SB MAP decoding. The decoding procedure of the reverse computations is illustrated in Fig. 4. Compared with the conventional decoding procedure shown in Fig. 3, the reverse decoding procedure adds a reversion checker, a reversion flag cache, and a reverse recursion processor (RRP). The reversion checker decides whether the 2^{v-1} state metrics computed by the NRP are reversible or not. If a state metric is not reversible, this state metric is stored in one subbank of the SMC. Meanwhile, the reversion flag cache stores the path information of this state metric. To compute the *a posteriori* LLR, the irreversible state metric is read out from the SMC according to the path information stored in the reversion flag cache. Otherwise, the reversible state metric is computed by the RRP, composed of 2^{v-1} reverse units. The recovered 2^{v-1} state metrics are recursively fed back to the RRP to calculate the next reversible state metrics. The reverse computations reduce the power consumption of the radix-2 SB MAP decoder because the subbanks of SMC are dynamically accessed, and the computational power of the reversion checker and RRP is small. The reverse computations for the radix-2 SB L-MAP decoding achieve an around 30% power reduction with an over 20% logic overhead. However, the reversion checker and reversion flag cache prolong the critical path or decoding cycles. In addition, dividing the SMC into subbanks increases the silicon area of the SMC and consumes more overall power of the SMC if all subbanks are accessed.

For the radix-2 SB MAP decoding, a 2^{v-1} -state trellis structure can be decomposed into 2^{v-2} radix-2 butterfly structures.

Fig. 5. Natural, reverse, and traceback recursions in the (a)–(c) radix-2 butterfly structures and (d)–(f) radix-4 butterfly structures. The symbol index is denoted by k . For the conventional decoding procedure, the computational units in (a) are the ACSUs. For the reverse decoding procedure, the computational units in (a) and (d) are the ACSUs and reversion checkers, and the computational units in (b) and (e) are the reverse units. For the traceback decoding procedure, the computational units in (a) and (d) are ACSUs only, and the computational units in (c) and (f) are the TBUs.

Fig. 5(a) and (b) illustrates an example of the SB reverse computation in a radix-2 butterfly structure. In Fig. 5(a), the reversion checker checks all fixed paths and determines the reversible paths. In Fig. 5(b), the dashed lines denote the reversible (selective) paths determined by the reversion flag cache. One radix-2 butterfly structure has four paths and four cases to be checked. The essential DB MAP decoding is radix-4 trellis decoding. For the radix-4 DB MAP decoding, a 2^{v-1} -state trellis structure can be decomposed into 2^{v-3} radix-4 butterfly structures. Fig. 5(d) and (e) illustrates an example of the DB reverse computation in a radix-4 butterfly structure. One radix-4 butterfly structure has 16 paths and 256 cases to be checked in the reverse computations. Hence, the reverse computations for the radix-4 trellis require more complicated reversion checkers and larger reversion flag caches. The computational complexities are dramatically increased when the reverse computations are extended from the SB to the DB MAP.

IV. PROPOSED MEMORY-REDUCED TRACEBACK MAP DECODING

Here, the traceback MAP decoding is proposed to reduce the power consumption of the SMC. The traceback MAP decoding has five major stages/phases, given here.

- 1) The branch metrics are computed with the received code-words and the *a priori* LLR in the natural order.
- 2) The forward (or backward) state metrics are recursively computed by the NRP with the branch metrics in the natural order, and the difference metrics are stored into the

Fig. 6. Traceback decoding procedure.

SMC. Note that the difference metric is the difference between two state metrics and has the same bit-length of the state metric.

- 3) The forward (or backward) state metrics are recursively traced back by the TRP with the stored difference metrics in the reverse order. Concurrently, the backward (or forward) state metrics are recursively computed with the branch metrics.
- 4) The *a posteriori* LLR is computed with regenerated forward (or backward) state metrics, the backward (or forward) state metrics, and branch metrics by the LAPO in the reverse order.
- 5) The extrinsic values and hard bits are computed in the reverse order with the *a posteriori* LLR.

In contrast to the conventional MAP decoding, the traceback MAP decoding reduces the number of stored metrics by accessing the difference metrics. Hence, the SMC power consumption is reduced. In addition, the computational power overhead of tracing the state metrics back is much smaller than the SMC power consumption. Thus, the overall power consumption of the MAP decoding is reduced. The work in [18] has introduced that not absolute values but differences between the state metrics are important for the *a posteriori* LLR. In the proposed traceback computation, the differences between state metrics are kept by storing the difference metrics. Hence, the traceback MAP decoding performs without losing correction ability. In addition, the proposed traceback computation works in the L-MAP and (E)ML-MAP.

Fig. 6 shows the proposed traceback decoding procedure, which is a modification of the conventional decoding procedure shown in Fig. 3. Compared with the conventional decoding procedure, only an additional TRP is added. Fig. 5(a) and (c) illustrates an example of the radix-2 SB traceback computation in a radix-2 butterfly structure. In Fig. 5(a), only one difference metric (black arc) computed by a radix-2 ACSU is stored in the SMC. In Fig. 5(c), the two state metrics (white nodes) are traced back in the traceback recursion by one traceback unit (TBU) with the stored difference metric (black arc). The recovered two state metrics are recursively fed back to the TRP to calculate the next two state metrics. The stored metrics are reduced from two state metrics to one difference metric. The bit-lengths of the state metric and difference metric are the same. Thus, the radix-2 traceback SB MAP decoding requires half the SMC size of the conventional decoding procedure. Compared with the reverse computations shown in Figs. 4 and

5(b), the traceback computation has fixed paths and requires no complicated checker and path selection.

The design details of the radix-2 traceback SB MAP decoding, including the radix-2 ACSU, radix-2 TBU, and overall architecture of the WCDMA CTC decoder, can be referred to in [19]. Based on the experimental results using a 0.18- μm CMOS process, the radix-2 SB traceback MAP decoding achieves a 21.4% power reduction of the SW L-MAP decoder with a 3.2% logic overhead.

V. TRACEBACK COMPUTATION AND COMPUTATIONAL UNITS FOR THE RADIX-4 DB MAP DECODING

In this paper, we emphasize the design of the radix-4 traceback DB MAP decoding and the corresponding computational units. Here, we demonstrate how the radix-4 traceback DB MAP decoding works with accessing the difference metrics. Two widely used ACSUs are then described, and the corresponding TBUs are proposed for the radix-4 traceback DB MAP decoding.

A. Traceback Computation for the DB MAP Decoding

The radix-4 traceback DB MAP decoding still employs the aforementioned five major stages/phases in Section IV and the traceback decoding procedure shown in Fig. 6. For the DB MAP decoding, the decoding trellis changes to the radix-4 trellis. Fig. 5(d) and (f) illustrates an example of the traceback computation in a radix-4 butterfly structure. In Fig. 5(d), the natural recursion in a radix-4 butterfly structure shows that three difference metrics (black arcs) are generated by a 4-input 1-output ACSU. These three difference metrics are stored into the SMC for the traceback computation. In Fig. 5(f), one 1-input 4-output TBU then traces the four state metrics (white nodes) back, with the three stored difference metrics (black arcs) in the traceback recursion.

Taking the DB RCS encoder shown in Fig. 2, for instance, Fig. 7(a) illustrates the corresponding eight-state radix-4 trellis diagram of the natural recursion for the DB MAP decoding, where t denotes the time index in the natural order, and k denotes the symbol index. Fig. 7(b) illustrates the radix-4 trellis of the traceback recursion for the DB MAP decoding, where t' denotes the time index in the reverse order. In the conventional decoding procedure (see Fig. 3), the eight states metrics are recursively computed by the NRP. The SMC stores these eight state metrics to compute the *a posteriori* LLR. In the traceback decoding procedure (see Fig. 6), the six difference metrics [black arcs in Fig. 7(a)] are computed by the NRP and stored into the SMC. The TRP, composed of 2 TBUs [black nodes in Fig. 7(b)], traces the eight state metrics back with the stored six difference metrics [black arcs in Fig. 7(b)]. Compared with the conventional decoding procedure, the stored metrics are reduced from eight state metrics to six difference metrics. Thus, the traceback computation reduces the SMC power consumption for the DB MAP decoding.

B. Radix-2 $\times$ 2 Traceback Pair

For the radix-4 MAP decoding, two types of ACSUs, the radix-2 $\times$ 2 ACSU and the radix-4 ACSU, are widely used to constitute the NRP. Fig. 8(a) shows an example of the

Fig. 7. 8-state radix-4 trellis diagrams of the (a) natural recursion and (b) traceback recursion. The symbol index is denoted by k . The time index in the natural recursion is denoted by t , and the time index in the traceback recursion is denoted by t' . The computational units in (a) are the ACSUs, and the computational units in (b) are the TBUs.

radix-2 $\times$ 2 ACSU. The radix-2 $\times$ 2 ACSU consists of four front adders, three radix-2 compare-select units (CSUs), and an LUT. In the proposed traceback computation, three difference metrics (Diff_0, Diff_1, and Diff_2) generated by three radix-2 CSUs are stored in the SMC. Fig. 8(b) shows the corresponding TBU of the radix-2 $\times$ 2 ACSU. Fig. 8(c) illustrates a computational example of the radix-2 $\times$ 2 ACSU and TBU. The radix-2 $\times$ 2 ACSU obtains the maximal state metric B based on Diff_0, Diff_1, and Diff_2. Subsequently, the radix-2 $\times$ 2 TBU regenerates A, B, C, and D based on Diff_0, Diff_1, and Diff_2, since B can be initially achieved. Hence, the four state metrics can be recomputed by the radix-2 $\times$ 2 TBU with the difference metrics stored in the SMC. In the radix-2 $\times$ 2 TBU, the sign bit of the difference metric decides the paths of the two multiplexers and the operation of the binary adder/subtractor. Taking the trellis diagram shown in Fig. 7(b), for instance, six difference metrics are stored in the SMC because two current states and two TBUs can trace eight next states back. The storage of the SMC is reduced from eight state metrics to six difference metrics at each stage. Note that the values A, B, C, and D in the output end of the radix-2 $\times$ 2 TBU can be the input values of the LAPO to compute $\Lambda_{\text{apo},k}^{(z)}$. This approach reduces eight adders ($(\alpha_k + \gamma_k)$ or $(\beta_k + \gamma_k)$ in (1d)) in the LAPO.

C. Radix-4 Traceback Pair

Fig. 9(a) shows an example of the radix-4 ACSU. The radix-4 ACSU has a comparator to select the maximal state metric quickly. Unlike the radix-2 $\times$ 2 ACSU, three difference metrics related to A (Diff_0, Diff_1, and Diff_2) and two selective bits (S0 and S1) of the radix-4 ACSU are stored in the SMC. The

Fig. 8. Radix-2 $\times$ 2 traceback pair: (a) the ACSU, (b) the TBU, and (c) a computational example.

corresponding TBU of the radix-4 ACSU is shown in Fig. 9(b). Fig. 9(c) illustrates a computational example of the radix-4 ACSU and TBU. The radix-4 ACSU obtains the maximal state metric B based on two selective bits generated by the six parallel subtractions in the comparator. The three difference metrics related to A are stored in the SMC. Since B can be initially achieved, A can be regenerated by the radix-4 TBU based on the stored S0 and S1. Subsequently, the radix-4 TBU regenerates A, B, C, and D based on Diff_0, Diff_1, and Diff_2. Taking the trellis diagram shown in Fig. 7(b), for instance, six difference metrics and four extra selective bits are stored in the SMC because two current states and two TBUs can trace eight

next states back. The storage of the SMC is reduced from eight state metrics to six difference metrics and four extra bits at each stage. The values A, B, C, and D in the output end of the radix-4 TBU can be the input values of the LAPO to compute $\Lambda_{apo,k}^{(z)}$ in. This approach reduces eight adders $[(\alpha_k + \gamma_k)]$ or $(\beta_k + \gamma_k)$ in (1d)] in the LAPO.

These two traceback pairs perform the (E)ML-MAP if the LUT of the corrective term in (3) is not implemented. Otherwise, these two traceback pairs perform the L-MAP. The proposed traceback computation and traceback pairs of the radix-4 DB MAP decoding can be simply applied to the radix-4 SB MAP decoding with a simple trellis modification.

Fig. 9. Radix-4 traceback pair: (a) the ACSU, (b) the TBU, and (c) a computational example.

VI. COMPARISONS AND EXPERIMENTAL RESULTS

Here, accurate silicon area and power evaluations are obtained by using Verilog HDL codes synthesized with the standard cell library of TSMC 0.13- μm CMOS process. The decoding procedures of the conventional and proposed traceback structures are only considered and evaluated in the radix-4 DB EML-MAP.

A. Area and Power Evaluations and Comparisons

Table I lists a summary of the conventional and traceback structures for the radix-4 DB EML-MAP decoding, where n_{sm} denotes the bit-length of a state metric or a difference metric. The constraint length v cannot be less than 3 for exploiting the radix-4 trellis. Taking $v = 4$ and $n_{\text{sm}} = 10$, for instance, eight radix-2 $\times$ 2 (or radix-4) ACSUs generate eight state metrics at each time stage. Hence, the SMC of the conventional structures has 80 bit-lengths. However, the traceback structure composed of eight radix-2 $\times$ 2 ACSUs and two radix-2 $\times$ 2 TBUs reduces the SMC bit-lengths from 80 to 60. The traceback structure composed of eight radix-4 ACSUs and two radix-4 TBUs reduces the SMC bit-lengths from 80 to 64.

For the comparison of the different structures, the practical evaluations are under the WiMAX CTC decoding. The D -type

TABLE I
SUMMARY OF THE CONVENTIONAL AND TRACEBACK STRUCTURES

Structure	SMC bit-length	NRP	TRP
Radix-2 $\times$ 2 Conventional	$2^{v-1} \times n_{\text{sm}}$	2^{v-1} ACSUs	-
Radix-4 Conventional	$2^{v-1} \times n_{\text{sm}}$	2^{v-1} ACSUs	-
Radix-2 $\times$ 2 Traceback	$2^{v-3} \times 3 \times n_{\text{sm}}$	2^{v-1} ACSUs	2^{v-3} TBUs
Radix-4 Traceback	$2^{v-3} \times (3 \times n_{\text{sm}} + 2)$	2^{v-1} ACSUs	2^{v-3} TBUs

parallel-window (PW) MAP decoding in [26] is adopted to achieve a high throughput rate because the decoding latency is 1 L . Table II lists evaluation parameters under the specification of WiMAX CTC. Ten parallel windows are used to decode an $N = 240$ CTC block, and we achieve $L = 24$. The size of information bits (B) is a double of a block size (N) because of the DB CTC. The bit-length of a state metric (α_k or β_k) or a difference metric is 10.

Table III shows the evaluated results of computational units of the different structures. The silicon area and path delay are reported by Synopsis Design Vision. The power consumption on 2-dB SNR noisy data is estimated by Synopsis PrimePower at 100 MHz operating frequency. For the eight-state radix-4 trellis, eight ACSUs (as an NRP) are grouped as two examples of the conventional structures. Eight ACSUs (as an NRP) and two

TABLE II
EVALUATION SPECIFICATION OF WiMAX CTC DECODING

Decoding Algorithm	PW EML-MAP ($\delta = 0.75$)
Information Bits (B)	480
Block Size (N)	240
Number of Iterations (Iter.)	4
Number of Parallel Window	10
Window Size (L)	24
Bit Error Rate	10^{-5}
Data Quantization (Total bits, Fractional bits)	$y_k^j : (5, 3)$ $\gamma_k^{(z)}, \Lambda_{ex,k}^{(z)}, \Lambda_{in,k}^{(z)} : (9, 3)$ $\alpha_k, \beta_k : (10, 3)$ $\Lambda_{apo,k}^{(z)} : (11, 3)$

TABLE III
COMPUTATIONAL UNIT COMPARISON OF THE DIFFERENT STRUCTURES

Structure	Unit	Path Delay (ns)	Area (μm^2)	Power (mW)
Radix-2 $\times$ 2 Conventional	NRP (8 ACSUs)	9.35	18540.70	0.65
Radix-4 Conventional	NRP (8 ACSUs)	5.77	22157.86	0.75
Radix-2 $\times$ 2 Traceback	NRP (8 ACSUs)	9.35	18540.70	0.65
	TRP (2 TBUs)	6.02	8276.52	0.08
Radix-4 Traceback	NRP (8 ACSUs)	5.77	22157.86	0.75
	TRP (2 TBUs)	5.51	5822.08	0.05

TBUs (as a TRP) are grouped as two examples of the traceback structures. The radix-2 $\times$ 2 ACSU has the longest path delay, because the values of the latter radix-2 CSU in the radix-2 $\times$ 2 ACSU are not correct until the sign (most significant) bits of the two former radix-2 CSU are stable. The radix-2 $\times$ 2 TBU does not suffer from this problem because the sign bits of the difference metrics are initially known. In addition, the radix-4 ACSU selects the maximal state metric quickly because the comparator generates selective bits based on the six parallel subtractions at the first level. Compared with the radix-2 $\times$ 2 traceback structure, the radix-4 traceback structure has shorter and more balanced path delays. However, the radix-2 $\times$ 2 traceback structure has less area costs and power consumptions. Because the ACSU dominate the operating frequency of a MAP decoder, the radix-4 traceback structure can derive a higher operating frequency than the radix-2 $\times$ 2 traceback structure. Operating at a higher operating frequency consumes more power for the radix-4 traceback structure. Thus, it is a tradeoff between the power consumption and maximum operating frequency for the radix-4 traceback DB MAP decoding.

In Table IV, the SMCs composed of single-port (SP) RAMs are generated by using the TSMC 0.13- μm process for the comparison of the different structures. Because of the D -type PW MAP decoding, the SMC can be implemented by a SP RAM with depth $L/2$. Note that eight state metrics have to be stored in the SMC, despite the conventional structure composed of the radix-2 $\times$ 2 or radix-4 ACSUs. For the radix-2 $\times$ 2 traceback structure, only six difference metrics are stored in the SMC. For the radix-4 traceback structure, six difference metrics and four

TABLE IV
SMC COMPARISON OF THE DIFFERENT STRUCTURES

Structure	SMC Size (Words $\times$ Bits)	Area (μm^2)	Power (mW)
Radix-2 $\times$ 2 Conventional	12 $\times$ 80	44061.11	2.20
Radix-4 Conventional	12 $\times$ 80	44061.11	2.20
Radix-2 $\times$ 2 Traceback	12 $\times$ 60	33075.37	1.65
Radix-4 Traceback	12 $\times$ 64	35417.95	1.77

extra selective bits are stored in the SMC. Fig. 10 shows comparisons of silicon area and power consumption of the SMC and TRP. The radix-2 $\times$ 2 traceback structure achieves a 24.9% area reduction and 25% power reduction of the SMC. On the other hand, the radix-4 traceback structure achieves a 19.6% area reduction of the SMC and 19.5% power reduction of the SMC. The power overhead of the TRPs is less than 4%, and the area overhead of the TRPs is less than 19%. Thus, the radix-4 and radix-2 $\times$ 2 traceback structure achieve the area and power reduction of the SMC of the radix-4 and radix-2 $\times$ 2 conventional structure.

B. Area and Power Evaluations of PW EML-MAP Decoders

Fig. 11 illustrates a processing element (PE) employing the traceback D -type PW EML-MAP decoding. The architecture can be divided into the forward recursion path (upper path) and backward recursion path (lower path). One branch metrics unit (BMU) for (1a), one NRP for (1b) or (1c), one SMC with depth $L/2$, one proposed TRP, one LAPO for (1d), one log-extrinsic module (LEX) for (1e), and one hard decision module (HD) for (2) are used for each path. When the TRPs are removed, the PE performs the conventional D -type PW EML-MAP decoding. The branch metrics are directly calculated without buffering in a branch metrics cache because of the D -type PW decoding. To meet the parameters in Table II, ten PEs are constructed as a DB MAP kernel.

Fig. 12 shows comparisons of silicon area and power consumption of the ten PEs composed of the conventional and traceback structures. The power consumption on 2-dB SNR noisy data is estimated at 100 MHz operating frequency. Compared with the radix-2 $\times$ 2 conventional structure, the radix-2 $\times$ 2 traceback structure achieves a 9.7% power reduction and a 2.1% area reduction. The logic overhead of radix-2 $\times$ 2 TRP is 9.8%. Similarly, the radix-4 traceback structure achieves a 7.9% power reduction and a 2.1% area reduction compared with the radix-4 conventional structure. The logic overhead of radix-4 TRP is 6.6%. The silicon areas of the traceback structures are not significantly reduced because the radix-4 DB MAP decoding complicates the hardware complexities of all computational units. Compared with the conventional structures, however, the power consumptions of the traceback structures are noticeably lower. The logic overhead of the radix-4 DB traceback computation is less than 10%.

VII. APPLICATION TO 12-MODE WiMAX CTC DECODER

Here, the 12-mode WiMAX CTC decoder for $N = 24$ –240 is presented. The design parameters of the CTC decoding are

Fig. 10. (a) Power consumption and (b) silicon area comparisons of the SMC and TRP using the conventional and traceback structures.

Fig. 11. Architecture of the processing element (PE) employing traceback PW EML-MAP decoding.

Fig. 12. (a) Power consumption and (b) silicon area comparisons of 10 PW EML-MAP PEs composed of the conventional and traceback structures.

shown in Table II. A prototyping CTC decoder has been implemented by using a TSMC 0.13- μ m CMOS process.

A. Overall Architecture

A VLSI architecture design of the 12-mode WiMAX CTC decoder has been presented in [27] to achieve the features of high throughput and efficient reconfigurability. The overall architecture of the implemented 12-mode WiMAX CTC decoder

is shown in Fig. 13. The decoder is composed of three input buffers, an internal buffer, an output buffer, a global controller, and a DB MAP kernel. The DB MAP kernel is composed of ten PW EML-MAP PEs and the conjoint WiMAX CTC interleavers (CIs). Because the radix-2x2 traceback structure has less power consumption (see Fig. 12), the radix-2x2 traceback structure is adopted in the PEs. Each buffer is divided into ten banks to be accessed simultaneously by the PE. To satisfy the

Fig. 13. Block diagram of the 12-mode WiMAX CTC decoder.

Fig. 14. Chip layout of the proposed 12-mode WiMAX CTC decoder. (+ represents the SMC composed of single-port RAM.)

power-efficient 12-mode CTC decoding, the global controller activates the appropriate PEs, CIs, and buffer banks, depending on the block size N .

B. Prototyping Chip Implementation

The chip layout and summary of the prototyping chip implemented by using the TSMC 0.13- μm CMOS process within a core size of 7.16 mm^2 are shown in Fig. 14 and Table V, respectively. The prototyping chip contains 27.4 Kb RAM and integrates 635 Kgates of logic. Each PE accounts for 52.3 Kgates of logic, and each CI accounts for 0.51 Kgates of logic. Based on worst-case static timing analysis and post-layout simulation results, the decoder achieves a maximum operating frequency of 100 MHz. The post-layout, gate-level, and typical-case (@1.2 V, 25 °C) power consumption of this CTC decoder is 197.3 mW, which is estimated at 100 MHz operating frequency on 2-dB SNR noisy data. For a single WiMAX FEC block within the 12 general transmissions, this CTC decoder can achieve a higher throughput rate of 115.4 Mbps at 100 MHz than that of 102.5 Mbps at 214 MHz of the Xilinx CTC decoder implemented in a FPGA [28].

C. Comparisons of CTC Decoders

In Table VI, the proposed 12-mode WiMAX CTC decoder is compared with other chip designs that support multiple block sizes. The work in [29] is designed for the HSDPA standard with

TABLE V
CHIP SUMMARY OF THE 12-MODE WiMAX CTC DECODER

Technology		TSMC 0.13 μm CMOS
Max. Frequency		100 MHz
Core Size		$2.58 \times 2.58 \text{ mm}^2$
Max. Power	@1.32V, -40°C	255.7 mW@100 MHz
	@1.2V, 25°C	197.3 mW@100 MHz
	@1.08V, 125°C	163.9 mW@100 MHz
Max. Throughput Rate		115.4 Mbps@100 MHz, 4 Iter.

Note that the evaluation is reported by post-layout simulations.

TABLE VI
COMPARISONS OF DIFFERENT CTC DECODER CHIPS

	Proposed*	[29]	[30]
Technology	0.13 μm	0.18 μm	0.18 μm
Core Voltage	1.2 V	1.8 V	1.8 V
Standard	WiMAX	HSDPA	-
Information Bits	48–480	40–5114	64–384
CTC Decoding	8-state, radix-4 DB	8-state, radix-4 SB	8-state, radix-2 SB
MAP PE	10 PW-EML MAP	1 SW-LMAP	7 SW-L-MAP
Iteration	4	6	4.43
Frequency	100 MHz	145 MHz	160 MHz
Core Area	6.66 mm^2	14.5 mm^2	7.16 mm^2
Logic Gate	635 Kgates	410 Kgates	373 Kgates
RAM Size	27.4 Kb	0.45 Mb	36 Kb
Throughput	115.4 Mbps	24 Mbps	71.7 Mbps
Power	197.3 mW	1450 mW	N/A
NEE	0.43 nJ/bit/Iter.	2.33 nJ/bit/Iter.	0.51 nJ/bit/Iter.
NAE	0.68 bits/ mm^2	0.12 bits/ mm^2	0.53 bits/ mm^2

* The evaluation is reported by post-layout simulations.

one radix-4 SB SW L-MAP PE and block sizes from 40 to 5114. The work in [30] is designed with seven radix-2 SB SW L-MAP PEs and block sizes from 64–384. It is hard to compare these chips since the coding parameters are different from each other. However, we use normalized energy efficiency (NEE)

$$\text{NEE} = \frac{\text{Power}}{\text{Throughput} \times \text{Iteration}} \times \text{Normalized energy factor} \quad (4)$$

as one performance index. The NEE indicates how much energy a decoder chip consumes to process a hard bit at an iteration. In addition, we use normalized area efficiency (NAE)

$$\text{NAE} = \frac{\text{Throughput}}{\text{Area} \times \text{Frequency}} \times \text{Normalized area factor} \quad (5)$$

as the other performance index. The NAE indicates how many hard bits per one mm^2 for a single CTC block a decoder chip decodes. When we normalize the works from 0.18- μm to 0.13- μm technology, the normalized energy factor is $0.23 = (1.2 \text{ V}/1.8 \text{ V})^2 \times (0.13 \mu\text{m}/0.18 \mu\text{m})^2$. Similarly, the normalized area factor is $1.92 = (0.18 \mu\text{m}/0.13 \mu\text{m})^2$. Our proposed decoder achieves a lower NEE (0.43 nJ/bit/iteration) and higher NAE (0.68 bits/ mm^2). Note that the NEE and NAE are not used to justify which design is superior to the others, but to provide an evaluative method for reference.

VIII. CONCLUSION

To reduce the power consumption of SMC, the traceback MAP decoding has been presented with a low logic overhead. The proposed traceback MAP decoding performs in the L-MAP and (E)ML-MAP without losing correction ability. Two pairs of the traceback computation are introduced for the radix-4 DB MAP decoding. The traceback radix- 2×2 pair has low hardware costs, and the radix-4 traceback pair has short path delays. In addition, the proposed traceback pairs of the radix-4 DB MAP decoding can be simply applied to the radix-4 SB MAP decoding. The experimental result shows that the two traceback structures achieve an around 20% power reduction of the SMC, and around 7% power reduction of ten DB MAP decoders for the WiMAX CTC. Compared with other designs, the 12-mode WiMAX CTC decoder employing the radix- 2×2 traceback structure achieves a low energy efficiency of 0.43 nJ/bit per iteration.

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