ADAPTIVE CHANNEL-SHORTENED INTERPOLATED ECHO AND NEXT CANCELLER DESIGNS APPLIED TO 10GBASE-T ETHERNET SYSTEM

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ABSTRACT

In this paper, new echo and NEXT cancellers are proposed for echo and NEXT cancellation in full-duplex digital transmission over 10GBASE-T system. The proposed cancellation schemes inherit the concept of the adaptive interpolated FIR (AIFIR)-based crosstalk canceller, where the long portion is modeled by an adaptive sparse FIR filter. Furthermore, we also employ the channel shortening technique to shorten the impulse response of crosstalk interference. Hence, the complexity of echo and NEXT cancellers can be greatly reduced. Simulations show that, with AIFIR and channel shortening, the new echo and NEXT cancellers still meet the SNR requirement in 10GBASE-T system and the complexity reduction of the proposed echo and NEXT canceller in arithmetic is about 45% and 37% respectively. The reduction of hardware complexity results in computationally efficient VLSI implementation of the echo and NEXT cancellers in 10GBASE-T system.

Key words: 10GBASE-T, echo canceller, NEXT canceller, channel shortening, Interpolated FIR.

I. INTRODUCTION

In this paper, we take 10GBASE-T Ethernet [1] as our target system. In order to achieve the low cost property of Ethernet, the goal of this paper is to lower the cost of 10GBase-T DSP baseband. However, in the 10GBase-T system, the data transmission is divided into four wire lines and all of the four wire pairs are full-duplex. The 10GBase-T transceiver must be capable of dealing with the interferences, such as echo, near-end crosstalk (NEXT), and far-end crosstalk (FEXT). Conventional echo cancellation scheme [2-4] adopts the concept that the echo canceller is an adaptive FIR filter to produce an echo replica. The received signal subtracts the echo replica to eliminate the echo interference, as shown in Fig. 1. In [5], IIR filter architecture designs are proposed as echo cancellers to reduce the cost of echo canceller. However, the adaptive IIR filter suffers from stability and slow convergence problems because the error surfaces for adaptive IIR filters may not be unimodal [6]. The architecture of the NEXT canceller is similar to that of an echo canceller except the transmitter is now replaced by another transmitter which incurs the NEXT interference.

In order to produce the echo replica, the impulse response of the echo canceller must be adapted to the echo impulse response. Thus, the complexity and cost of echo canceller are proportional to the length of echo impulse response. However, in the 10GBASE-T environment, the echo impulse response is very long. Implementing the echo canceller requires the adaptive FIR filter with hundreds of taps. Therefore, the echo and NEXT cancellers, which are hundreds of taps, dominate the cost of 10GBase-T baseband DSP. In this paper, new echo and NEXT cancellers are proposed. We employ the channel shortening technique [12-14] to shorten the echo and NEXT responses, and use adaptive interpolated-FIR (AIFIR) architectures [8-11] to greatly reduce the hardware complexity. From system simulation results and cost analysis, the hardware cost savings of the proposed echo and NEXT cancellation schemes in arithmetic are about 45% and 37% respectively with only little performance degradation.

This paper is organized as follows. In section II, we
review several existing cost-reduction canceller designs. New canceller architectures and algorithms are derived in section III. In section IV, we apply the proposed schemes to 10GBASE-T Ethernet application and show the simulation results and hardware cost comparison. Finally, section IV concludes the work of this paper.

II. REVIEW OF EXISTING COST-REDUCTION WORKS

A. Adaptive Interpolated FIR Filter

One of the most computationally efficient implementations for narrow-band finite impulse response (FIR) filters is the interpolated FIR (IFIR) structure [7]. Fig. 2 shows the block diagram of an IFIR filter. The IFIR filter \( H(z) \) in \( z \) domain is given by

\[
H(z) = F(z^L)G(z),
\]

where \( L \) is the interpolation factor. \( F(z^L) \) and \( G(z) \) are described by:

\[
F(z^L) = \sum_{j=0}^{N_F-1} f_{4L} z^{-jL}, \quad G(z) = \sum_{i=0}^{N_G-1} g_{i} z^{-i},
\]

where \( N_F \) is the number of the nonzero taps of the filter \( F(z^L) \), and \( N_G \) is the length of the filter \( G(z) \). Here, \( F(z^L) \), is called the shaping filter with only every \( L \)th sample being nonzero. Because \( F(z^L) \) has a very sparse impulse response, the number of arithmetic operations can be reduced greatly. The second FIR filter, \( G(z) \), is a short-length interpolator filter which generates the missing samples by interpolation. Instead of generating all samples independently, we can design a decimated version of the filter, followed by an interpolator to generate other samples by interpolating between the existing samples. Typically, an IFIR filter requires approximately \( 1/L_{th} \) of the multipliers and adders of a conventional equivalent FIR filter [8].

A typical echo response, shown in Fig. 3, consists of a short duration main section with wide variations followed by a long duration tail section similar to a slowly decaying exponential. In order to reduce the computational complexity of the echo canceller, a two-stage echo canceller was proposed in [8][9] as shown in Fig. 4. The first stage is the main echo canceller (MEC) that is used to cancel the main section of the echo response while the second stage, the tail echo canceller (TEC), is used to cancel the tail section of the echo response.

Due to the general nature of the main echo section, an adaptive direct-form FIR filter is employed in the MEC. However, an adaptive interpolated FIR (AIFIR) filter is employed in the TEC due to the narrowband nature of the tail echo section. The two-stage echo canceller has been shown to provide significant hardware cost savings compared to the direct-form FIR echo canceller.

In [10][11], the authors claimed that the FIR and IFIR filters should be overlapped instead of being directly cascaded. Some echo responses in the overlapping region will be simultaneously cancelled by the FIR and IFIR filters to obtain better cancellation performance. Besides, in order to speed up the convergence speed, the authors also proposed a coefficient-nulling scheme to null some tap-weights in the FIR filter. Two schemes are illustrated in Fig. 5.

![Block diagram of an IFIR filter](image-url)

**Fig. 2** Block diagram of interpolated FIR filter.

![Typical echo response](image-url)

**Fig. 3** Typical echo response.

![The AIFIR-based echo canceller](image-url)

**Fig. 4** The AIFIR-based echo canceller.
B. Channel Shortening Technique

[13] reduces the cost of the echo canceller by employing the concept of channel shortening. In Fig. 6(a), a shortened impulse response filter (SIRF) is implemented at the echo path. The goal of SIRF is to shorten the echo impulse response to reduce the cost of the echo canceller. Thus, the effective echo channel can be modeled as

$$h_{\text{eff}}(k) = h(k) * p(k),$$

where \(k\) denotes the time-domain index. Generally speaking, the length of the effective echo channel is greater than that of the original echo channel since the nature of the convolution operation. However, if we constrain most of the energy of the effective echo channel in consecutive \(\nu\) taps and assume \(\nu\) is smaller than the length of the original channel, the channel shortening is achieved as shown in Fig. 6(b). Besides, because the largest \(\nu\) samples will not necessarily begin with the first samples, a delay parameter \(d\) is induced by the effective echo response. We can use the delay parameter \(d\) to indicate the start of the largest \(\nu\) samples. Therefore, the echo canceller can cancel the effective echo response correctly.

III. PROPOSED COST-EFFECTIVE ECHO AND NEXT CANCELLATION SCHEMES

In this section, we propose two new cancellation schemes. Both the schemes can be used to greatly reduce the complexity of the echo canceller as well as the NEXT canceller. Fig. 7(a) and Fig. 7(b) show the NEXT and echo responses, respectively. As we can see, the two responses are similar to each other. Wide magnitude variation appears in one short portion of the overall re-
spontaneous while narrow-band nature appears in other long regions of the overall response. Therefore, for the convenience of conveying our ideas, we take the echo response in Fig. 7(b) as our design example.

A. Proposed Two-Sided AIFIR Cancellation Scheme

Fig. 7(b) shows the echo impulse response in 10GBASE-T system. We can find that the echo response is something different to the typical echo response in Fig. 3. The short duration main section with wide variations appears approximately in the middle region of the total echo response. Thus, the two-stage echo canceller is not the most cost-effective solution in the 10GBASE-T system. From Fig. 7(b), we can divide the echo response into three sections. Two long durations, the head and tail sections, are similar to a slowly decaying exponential. One short duration, the main section, is rapidly changing. In this paper, a two-sided AIFIR echo canceller is proposed. The left side is the head echo canceller (HEC) that is used to simulate the head section. The middle section is the main echo canceller (MEC) that is used to simulate the main section. And the right side, the tail echo canceller (TEC), is used to simulate the tail section. Due to the general nature of the main echo section, an adaptive direct-form FIR is applied in the MEC. Nevertheless, due to the narrow-band nature of the head and tail sections, two AIFIR filters are employed in the HEC and TEC, respectively.

The proposed two-sided echo canceller architecture is shown in Fig. 8. The HEC, an AIFIR filter, consists of an interpolation filter $G_1(z)$ and an $L_1$-sparse adaptive FIR filter, where $L_1$ denotes the interpolation factor. The term, $L_1$-sparse, indicates that $(L_1-1)$ null taps are inserted between every two successive taps. Besides, the TEC is another AIFIR filter consisting of an interpolation filter $G_2(z)$ and a $L_2$-sparse adaptive FIR filter, where $L_2$ denotes the interpolation factor. The term, $L_2$-sparse, indicates that $(L_2-1)$ null taps are inserted between every two successive taps. The $D_1$ delays can be used to align the MEC to accurately simulate the main section of the echo response. Hence, the value of $D_1$ equals the length of the head section of the echo response. Furthermore, the $D_2$ delays can be used to align the TEC to accurately simulate the tail section of the echo response. Hence, the value of $D_2$ equals the length of the main section of the echo response.

The equations describing the two-sided AIFIR echo canceller are summarized below.

$$\hat{y}(k) = C^T(k)A(k) + D^T(k)B(k) + W^T(k)X_N(k - D_1)$$ (4a)

$$e(k) = y(k) - \hat{y}(k)$$ (4b)

$$C(k + 1) = C(k) + \mu_e e(k)A(k)$$ (4c)

$$D(k + 1) = D(k) + \mu_d e(k)B(k)$$ (4d)

$$W(k + 1) = W(k) + \mu_w e(k)X_N(k - D_1)$$ (4e)

where

$W(k) = [w_1(k) , w_2(k) , \ldots , w_N(k)]^T$

$N \times 1$ vector of coefficients of the main echo canceller

$C(k) = [c_1(k) , c_2(k) , \ldots , c_N(k)]^T$

$N_1 \times 1$ vector of non-zero coefficients of the $L_1$-sparse adaptive FIR

$D(k) = [d_1(k) , d_2(k) , \ldots , d_N(k)]^T$

$N_2 \times 1$ vector of non-zero coefficients of the $L_2$-sparse adaptive FIR

$X_N(k-D_1) = [x(k-D_1) , x(k-D_1-1) , \ldots , x(k-D_1-1+N-1)]^T$

$N \times 1$ vector of inputs of the main echo canceller

$A(k) = [a_1(k) , a_2(k-L_1) , \ldots , a_N(k-(N_1-1)L_1)]^T$

$N_1 \times 1$ vector of effective inputs of the $L_1$-sparse adaptive FIR

$B(k) = [b_1(k) , b_2(k-L_2) , \ldots , b_N(k-(N_2-1)L_2)]^T$

$N_2 \times 1$ vector of effective inputs of the $L_2$-sparse adaptive FIR

$\hat{y}(k)$ The output of the two-sided AIFIR echo canceller

$e(k)$ Estimation error

$\mu$ Adaptation step size

Based on our proposed two-sided AIFIR echo canceller, we also adapt the overlapping and the coefficient-nulling schemes employed in [11]. First, the overlapping scheme is listed as follows:

$$N_{G1} = 2S_1L_1 - 1$$ (5a)

$$N_{G2} = 2S_2L_2 - 1$$ (5b)

$$N_{o1} = N_{G1} - L_1$$ (5c)

$$N_{o2} = N_{G2} - L_2$$ (5d)

$$N = D_2 + N_{o1} + N_{o2}$$ (5e)

where $N_{G1}$ and $N_{G2}$ represent the number of taps of the two interpolation filters $G_1$ and $G_2$, respectively. $S_1$ is the
number of the tap-weights in the interpolation filter \( G_1 \) involved in calculating an interpolated value for a single side span, and \( S_2 \) is the number of the tap-weights in the interpolation filter \( G_2 \) involved in calculating an interpolated value for a single side span. \( N_{o1} \) is the overlapped taps for the HEC and the MEC, and \( N_{o2} \) is the overlapped taps for the TEC and the MEC. Therefore, the increased number of tap-weights in the MEC is \( N_{o1}+N_{o2} \). Second, some tap-weights in the main echo canceller should be nulled. The coefficient-nulling scheme is listed as follows:

\[
\begin{align}
[w_{L_1}(k), w_{2L_1}(k), \ldots, w_{(S_1 - 1)L_1}(k)]^T &= 0_{S_1} \quad (6a) \\
[w_{N-(S_1-1)L_1}(k), w_{N-(S_2-1)L_2+1}(k), \ldots, w_{N-L_2+1}(k)]^T &= 0_{S_2} \quad (6b)
\end{align}
\]

where \( 0_{S_1} \) and \( 0_{S_2} \) represent \((S_1-1)\times1\) and \((S_2-1)\times1\) zero vectors, respectively.

Because of applying overlapping schemes, the delay values in Fig. 8 should be modified as follows:

\[
\begin{align}
D'_1 &= D_1 - N_{o1} \quad (7a) \\
D'_2 &= D_2 - N_{o2} \quad (7b)
\end{align}
\]

B. Proposed Channel-Shortening-Based AIFIR Cancellation Scheme

In order to further reduce the complexity of the two-sided echo canceller, we also apply the channel shortening technique to the echo response [13]. Fig 7(c) is the echo impulse response after channel shortening which shows two important properties. First, the length of the main section is shorter than that of the main section of the original echo response in Fig. 7(b). Thus, we can use a lower-order direct-form FIR filter in the MEC. Second, the magnitude of the head section echo response of the shortened channel is too small so that it doesn’t need to implement AIFIR in the head section. In addition, it has been shown that the performance loss is negligible [13]. Therefore, it is only necessary to apply one-sided AIFIR for the tail section. Notice that although the total length of the tail section becomes greater, the hardware increment is negligible owing to the fact that the AIFIR filters are applied in the TEC.

The proposed channel-shortening-based AIFIR echo canceller architecture is shown in Fig. 9. A SIRF is used to shorten the echo response. The TEC, an AIFIR filter, consists of an interpolation filter \( G_3(z) \) and an \( L_3 \)-sparse adaptive FIR filter, where \( L_3 \) denotes the interpolation factor. The term, \( L_3 \)-sparse, indicates that \((L_3-1)\) null taps are inserted between every two successive taps. The \( D_3 \) delays can be used to align the MEC to accurately simulate the main section of the shortened echo response. Hence, the value of \( D_3 \) equals the length of the head section of the shortened echo response. Furthermore, the \( D_3 \) delays can be used to align the TEC to accurately simulate the tail section of the shortened echo response. Hence, the value of \( D_4 \) equals the length of the main section of the shortened echo response.

The equations describing the channel-shortening-based AIFIR echo canceller are summarized below.

\[
y(k) = P^T T(k) \quad (8a) \\
\hat{y}(k) = U^T(k) Q(k) + W^T(k) X_N(k - D_1) \quad (8b) \\
e(k) = y(k) - \hat{y}(k) \quad (8c) \\
U(k + 1) = U(k) + \mu_n e(k) Q(k) \quad (8d) \\
W(k + 1) = W(k) + \mu_n e(k) X_N(k - D_2) \quad (8e)
\]

where

\[
\begin{align}
W(k) &= [w_1(k), w_2(k), \ldots, w_N(k)]^T \\
U(k) &= [u_1(k), u_2(k), \ldots, u_{N_3}(k)]^T \\
P &= [p_1, p_2, \ldots, p_M]^T \\
X_N(k - D_3) &= [x(k - D_3), x(k - D_3 - 1), \ldots, x(k - D_3 - N + 1)]^T \\
Q(k) &= [q(k), q(k - L_3), \ldots, q(k - (N_3 - 1)L_3)]^T \\
T(k) &= [\tau(k), \tau(k - 1), \ldots, \tau(k - M + 1)]^T \\
\hat{y}(k) &= \text{The output of the channel-shortening-based AIFIR echo canceller} \\
e(k) &= \text{Estimation error} \\
\mu &= \text{Adaptation step size}
\end{align}
\]

In this design, we can also apply the overlapping and the coefficient-nulling schemes. First, we list the overlapping scheme as follows:

![Fig. 9 Block diagram of the proposed channel-shortening-based AIFIR echo canceller.](image-url)
\[ N_{G3} = 2L_3S_3 - 1 \]  
\[ N_{o3} = N_{G3} - L_3 \]  
\[ N = D_4 + N_{o3} \]

where \( N_{G3} \) represents the number of taps of the interpolation filter \( G_3 \), \( S_3 \) is the number of the tap-weights in this interpolation filter involved in calculating an interpolated value for a single side span. \( N_{o3} \) is the overlapped taps for the tail echo canceller and the main echo canceller. Therefore, the increased number of tap-weights in the main echo canceller is \( N_{o3} \). Second, some tap-weights in the main echo canceller should be nulled. The coefficient-nulling scheme is listed as follows:

\[
[w_{y-(S_3-1)L_3+t}(k), w_{y-(S_3-2)L_3+t}(k), \ldots, w_{y-L_3+t}(k)]^T = \theta_{S3}
\]

where \( \theta_{S3} \) represents \((S_3-1) \times 1\) zero vector.

It should be noted that although we apply overlapping schemes, the delay values in Fig. 9 keeps unchanged.

IV. PERFORMANCE ANALYSIS AND COST COMPARISON

In this section, we compare the conventional architectures, [11], and the proposed architectures. The simulation results show that the complexity reduction of the proposed architecture is the greatest among these architectures.

A. Floating-Point System Analysis

In the simulations, we apply the proposed echo and NEXT cancellation schemes to 10 Gigabit Ethernet applications. In 10GBASE-T systems, it achieves 10Gbps full-duplex transmission over 4 unshielded twisted pair (UTP) copper lines. The line coding is 16-level-pulse amplitude modulation (PAM16) over the UTP cat. 6. The cable length is 55m. Besides, in the channel equalization schemes, Tomlinson-Harashima Precoding (THP) is used to eliminate the post-cursor Intersymbol-Interference (ISI), while a feedforward equalizer (FFE) is used to eliminate the pre-cursor ISI. The channel impairments that we consider here are the insertion loss, echo responses and NEXT responses available from the IEEE 802.3an website [1]. We assume the receiver can operate in the correct sampling phase. The proposed channel-shortening-based AIFIR transceiver architecture is shown in Fig. 10. For each line, we add a SIRF at the receiver to jointly shorten the echo and NEXT responses, and place the proposed echo and NEXT cancellers in the system. We add AWGN with 30dB SNR to model the interferences and noises other than echo and NEXT. The comparison of the equalizer output mean square error (MSE) with different structures of the echo canceller is shown in Table 1 and the comparison of the equalizer output MSE with different structures of the NEXT canceller is show in Table 2. We perform 200 randomly independent rounds and average the results. Comparing the performance of the conventional architecture with the proposed architecture, we just have a little performance degradation in output with great complexity reduction. The performance of the proposed architecture can still meet the SNR requirement specified in 10GBASE-T.

B. Implementation Cost Comparison

For an \( N \)-tap adaptive FIR filter with interpolation factor \( L \), the required MACs are

\[
\text{Arithmetic} = \frac{N}{L} + \frac{N}{L}, \quad (11)
\]

In (11), the first term \( N/L \) represents the complexity of the filter, while the second term \( N/L \) represents the complexity of the weight update. Given an interpolation factor \( L \), we can calculate the number of effective tap weights in an AIFIR filter.

Table 3 shows the complexity comparison of the echo cancellers applied to 10GBASE-T systems. Compared with the conventional echo architecture in arithmetic, the cost savings of [11], two-sided echo cancellation scheme, and channel-shortening-based AIFIR echo cancellation scheme are 21.5%, 25.6% and 45.5%, respectively. Besides, Table 4 shows the complexity comparison of the NEXT cancellers applied to 10GBASE-T systems. Compared with the conventional NEXT architecture in arithmetic, the cost savings of [11], two-sided NEXT cancellation scheme, and channel-shortening-based AIFIR NEXT cancellation scheme are 21.5%, 25.6% and 45.5%, respectively.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>MSE(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>-26.93 dB</td>
</tr>
<tr>
<td>Two-sided AIFIR</td>
<td>-26.55 dB</td>
</tr>
<tr>
<td>Channel-shortening + AIFIR</td>
<td>-26.75 dB</td>
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Table 2  NEXT canceller output MSE of each architecture.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>MSE(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>-26.72 dB</td>
</tr>
<tr>
<td>Two-sided AIFIR</td>
<td>-26.31 dB</td>
</tr>
<tr>
<td>Channel-shortening + AIFIR</td>
<td>-26.51 dB</td>
</tr>
</tbody>
</table>
Fig. 10  The proposed transceiver architecture of 10GBASE-T system.

Table 3  Complexity comparison of echo canceller (EC).

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<tbody>
<tr>
<td>MEC</td>
<td>1000</td>
<td>678</td>
<td>569</td>
<td>398</td>
</tr>
<tr>
<td>HEC</td>
<td>-</td>
<td>-</td>
<td>38</td>
<td>-</td>
</tr>
<tr>
<td>TEC</td>
<td>-</td>
<td>84</td>
<td>64</td>
<td>104</td>
</tr>
<tr>
<td>Interpolator</td>
<td>-</td>
<td>23</td>
<td>46</td>
<td>23</td>
</tr>
<tr>
<td>SIRF</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>Total</td>
<td>1000</td>
<td>785</td>
<td>744</td>
<td>545</td>
</tr>
<tr>
<td>Saving</td>
<td>-</td>
<td>21.5%</td>
<td>25.6%</td>
<td>45.5%</td>
</tr>
</tbody>
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Table 4  Complexity comparison of NEXT canceller (NC).

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<tbody>
<tr>
<td>MNC</td>
<td>600</td>
<td>418</td>
<td>338</td>
<td>298</td>
</tr>
<tr>
<td>HNC</td>
<td>-</td>
<td>-</td>
<td>38</td>
<td>-</td>
</tr>
<tr>
<td>TNC</td>
<td>-</td>
<td>48</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>Interpolator</td>
<td>-</td>
<td>23</td>
<td>46</td>
<td>23</td>
</tr>
<tr>
<td>SIRF</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>Total</td>
<td>600</td>
<td>489</td>
<td>440</td>
<td>375</td>
</tr>
<tr>
<td>Saving</td>
<td>-</td>
<td>18.5%</td>
<td>24%</td>
<td>37.5%</td>
</tr>
</tbody>
</table>

Based AIFIR NEXT cancellation scheme are 18.5%, 24% and 37.5%, respectively. Therefore, among these architectures, the proposed two echo and NEXT cancellers have better cost-saving efficiency.

V. CONCLUSION

In this paper, we propose low-complexity echo and NEXT cancellation schemes for 10GBase-T Ethernet system. First, we use the two-sided AIFIR scheme to reduce the hardware complexity. In order to further reduce the hardware complexity, we use a SIRF to shorten the echo and NEXT responses and combine it with AIFIR. Simulation results show that with a little performance degradation, hardware complexity can be greatly reduced by the proposed schemes. The reduction of hardware complexity brings computationally efficient VLSI implementation of the echo and NEXT cancellers in 10GBASE-T Ethernet system.

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