A fast convergent pipeline adaptive decision feedback equalizer using a post-cursor processing filter is disclosed, which includes a feed-forward equalizer, a post-cursor processing filter, an adder, a slicer, a register, a pipelined feedback equalizer, a subtractor and an updating device. The pipelined feedback equalizer has a delay device coupled to the register for delaying its output signal, and a feedback equalizer coupled to the delay device for eliminating the post-cursor of the output signal. By using the post-cursor processing filter (PCF), it increases the operating clock rate with arbitrary speedup factor, and improves the convergence rate of the overall system.

8 Claims, 11 Drawing Sheets
FIG. 1 (PRIOR ART)
FIG. 2  (PRIOR ART)
FIG. 4
<table>
<thead>
<tr>
<th>channel I</th>
<th>$N_f$</th>
<th>$N_s$</th>
<th>$N_p$</th>
<th>Step Size</th>
<th>Other parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial ADFE</td>
<td>6</td>
<td>3</td>
<td>0</td>
<td>$2^{-7}$</td>
<td>$D_1=D_2=D_3=0$, LA=0, D_4=1, D_6=4</td>
</tr>
<tr>
<td>PIPEADFE</td>
<td>12</td>
<td>9</td>
<td>0</td>
<td>$2^{-7}$</td>
<td>$D_2=2D_1=12$, D_3=3, LA=0, D_4=1, D_6=4</td>
</tr>
<tr>
<td>PCFADFE</td>
<td>6</td>
<td>9</td>
<td>7</td>
<td>$2^{-7}$</td>
<td>$D_2=4D_1=2D_5=24$, D_3=3, LA=0, D_4=1, D_6=4</td>
</tr>
</tbody>
</table>

**FIG. 5 A**

<table>
<thead>
<tr>
<th>channel II</th>
<th>$N_f$</th>
<th>$N_s$</th>
<th>$N_p$</th>
<th>Step Size</th>
<th>Other parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial ADFE</td>
<td>7</td>
<td>3</td>
<td>0</td>
<td>$2^{-6}$</td>
<td>$D_1=D_2=D_3=0$, LA=0, D_4=1, D_6=7</td>
</tr>
<tr>
<td>PIPEADFE</td>
<td>13</td>
<td>9</td>
<td>0</td>
<td>$2^{-6}$</td>
<td>$D_2=2D_1=12$, D_3=3, LA=0, D_4=1, D_6=7</td>
</tr>
<tr>
<td>PCFADFE</td>
<td>7</td>
<td>9</td>
<td>7</td>
<td>$2^{-6}$</td>
<td>$D_2=4D_1=2D_5=24$, D_3=3, LA=0, D_4=1, D_6=7</td>
</tr>
</tbody>
</table>

**FIG. 5 B**
<table>
<thead>
<tr>
<th>channel III</th>
<th>N_f</th>
<th>N_p</th>
<th>Step Size</th>
<th>Other parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial ADFE</td>
<td>14</td>
<td>8</td>
<td>2^-7</td>
<td>D_1 = D_2 = D_3 = 0, L_A = 0, D_4 = 1, D_6 = 12</td>
</tr>
<tr>
<td>PIPE ADFE</td>
<td>20</td>
<td>14</td>
<td>2^-7</td>
<td>D_2 = 2D_1 = 12, D_3 = 3, L_A = 0, D_4 = 1, D_6 = 12</td>
</tr>
<tr>
<td>PCF ADFE</td>
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<td>14</td>
<td>2^-7</td>
<td>D_2 = 4D_1 = 2D_3 = 24, D_3 = 3, L_A = 0, D_4 = 1, D_6 = 12</td>
</tr>
</tbody>
</table>

FIG. 5C
The learning curve of PIPEADFE, PCFADFE and serial ADFE for channel 1

FIG. 6A
The learning curve of PIPEADFE, PCFADFE and serial ADFE (channel III)

FIG. 6B
The learning curve of PIPEADFE, PCFADFE and serial ADFE (channel II)

FIG. 6C
<table>
<thead>
<tr>
<th>speedup</th>
<th>Mult. in FFE and PCF</th>
<th>Mult. in FBE</th>
<th>Total adder</th>
<th>Mult. in FFE and PCF</th>
<th>Mult. in FBE</th>
<th>Total adder</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIPEADFE</td>
<td>2N_f + 2</td>
<td>2N_b</td>
<td>2(N_f + N_b + N) - 3</td>
<td>2N_f + 2</td>
<td>2N_b</td>
<td>2(N_f + N_b + N) - 3</td>
</tr>
<tr>
<td>PCFADFE</td>
<td>2(N_f + N - 1)</td>
<td>2N_b</td>
<td>2(N_f + N - 1)</td>
<td>2N_b</td>
<td>2(N_f + N - 1)</td>
<td>2(N_f + N_b + N) - 3</td>
</tr>
</tbody>
</table>

FIG. 8
FAST CONVERGENT PIPELINED ADAPTIVE DECISION FEEDBACK EQUALIZER USING POST CURSOR PROCESSING FILTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the technical field of adaptive decision feedback equalizer (ADFE) and, more particularly, to a fast convergent pipelined adaptive decision feedback equalizer (PADFE) using post-cursor processing filter (PCF), which is capable of eliminating the intersymbol interference (ISI) in input samples.

2. Description of Related Art

Conventionally, the adaptive decision feedback equalizer (ADFE) using Least Mean-Squared (LMS) algorithm is one of the key techniques in many magnetic storage and digital communication applications. Fig. 1 shows a block diagram of a serial adaptive decision feedback equalizer 100 (ADFE). As shown, in the serial ADFE 100, a feed-forward equalizer (FFE) 110 is provided for receiving the input samples x(n) and eliminating pre-cursor of the input samples x(n). An adder 150 adds the output signal of the FFE 110 and a feedback signal to produce an pre-quantization signal. A slicer 130 quantizes the pre-quantization signal and produces a white quantized signal. A register 140 is coupled to the slicer 130 for holding the white quantized signal. A feedback equalizer (FBE) 120 is provided for eliminating the post-cursor of the white quantized signal and producing the feedback signal. A subtractor 160 subtracts the pre-quantization signal from the quantized signal to produce a cost signal. An updating device 170 updates coefficients of the FFE 110 and FBE 120 based on the cost signal.

The updating mechanism of the serial ADFE 100 is based on the least mean square (LMS) error algorithm. The corresponding equations of the LMS-based serial ADFE 100 can be described as follows:

\[
\begin{align*}
\alpha(n) &= \alpha(n) + \alpha(n), \\
X(n) &= x(n) \ldots x(n-N_p), \\
Y(n) &= \hat{\alpha}(n-1) x(n-1) + \ldots + \hat{\alpha}(n-N_p) x(n-N_p), \\
\alpha_p(n) &= \sum_{m=1}^N a(n-D_m) X(n), \\
\hat{\alpha}(n) &= \sum_{m=1}^N \hat{\alpha}(n-m) Y(n), \\
\hat{\alpha}(n) &= \sum_{m=1}^N \hat{\alpha}(n-m) Y(n), \\
C(n) &= C(n) + \mu \sum_{m=1}^{1+N_p} (n-D_m-1) X(n-D_m-1), \\
D(n) &= D(n) + \mu \sum_{m=1}^{1+N_p} (n-D_m-1) Y(n-D_m-1),
\end{align*}
\]

The pipelined adaptive decision feedback equalizer (PAPIDFE) 200 maintains the functionality in the statistical behavior instead of input-output behavior by using the relaxed look-ahead technique. However, it suffers from some performance degradation such as output SNR and convergence rate. Although, the operating clock rate of the PAPIDFE 200 is larger than the ADFE 100. But the convergence rate of PAPIDFE 200 is quite slower than the ADFE 100. Therefore, there is a need to have a novel design of pipeline adaptive decision feedback equalizer that can mitigate and/or obviate the aforementioned problems.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a fast convergent pipelined adaptive decision feedback equalizer using a post-cursor processing filter for eliminating the inter-symbol interference (ISI) in input samples, so as to increase operating clock rate and convergence rate of overall system.

To achieve the aforementioned object, there is provided a fast convergent pipelined adaptive decision feedback equalizer using a post-cursor processing filter, which comprises a feed-forward equalizer, a post-cursor processing filter, an adder, a slicer, a register, a pipelined feedback equalizer, a subtractor and an updating device. The feed-forward equalizer is provided for receiving input samples and eliminating pre-cursor of the input samples. The post-cursor processing filter is coupled to the feed-forward equalizer for producing an output signal. The adder is provided for adding the output signal of the post-cursor processing filter and a feedback signal to produce an pre-quantization signal. The slicer is coupled to the adder for quantizing the pre-quantization signal and producing a white quantized signal. The register
is coupled to the slicer for holding the white quantized signal. The pipelined feedback equalizer has plurality of pipeline stages and is coupled to the register for eliminating the post-cursor of the white quantized signal and producing the feedback signal. The subtractor is provided for subtracting the pre-quantization signal from the quantized signal to produce a cost signal. The updating device is provided for updating coefficients of the feed-forward equalizer and pipelined feedback equalizer based on the cost signal and updating coefficients of the post-cursor processing filter based on the cost signal and the white quantized signal.

Other objects, advantages, and novel features of the invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of a conventional serial adaptive decision feedback equalizer (ADFE);

FIG. 2 shows a block diagram of a conventional pipeline adaptive decision feedback equalizer (PIPEADFE);

FIG. 3 shows a block diagram of a fast convergent pipelined adaptive decision feedback equalizer using a post-cursor processing filter (PCFADFE) in accordance with the present invention;

FIG. 4 shows an embodied circuit with a speedup factor of three in accordance with the present invention;

FIGS. 5(a)–(c) show parameter tables for simulation of channel I, II, and III, respectively;

FIGS. 6(a)–(c) show simulation results according to the parameters in FIG. 5, respectively;

FIG. 7 shows the output SNR of PIPEADFE and PCFADFE vs. speedup factor; and

FIG. 8 shows the hardware complexity of PIPEADFE and PCFADFE in speedup factor being equal to 2 and N.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference to FIG. 3, there is shown a functional block diagram of a fast convergent pipelined adaptive decision feedback equalizer using post-cursor processing filter 300 (PCFADFE) according to the present invention, which includes a feed-forward equalizer 310, a post-cursor processing filter 320, an adder 330, a slicer 340, a register 350, a pipelined feedback equalizer 360, a subtractor 370, and an updating device 380. The feed-forward equalizer 310 receives the input samples x(n) and eliminates pre-cursor of the input samples x(n). The post-cursor processing filter 320 is coupled to the feed-forward equalizer 310 and produces an output signal. The adder 330 adds the output signal of the post-cursor processing filter 320 and a feedback signal to produce a pre-quantization signal. The slicer 340 is coupled to the adder 330 for quantizing the pre-quantization signal and producing a white quantized signal. The register 350 is coupled to the slicer 340 for holding the white quantized signal. The pipelined feedback equalizer 360 includes a delay device 361 coupled to the register 350 for delaying the white quantized signal, and a feedback equalizer 362 coupled to the delay device 361 for eliminating the post-cursor of the white quantized signal and producing the feedback signal. The subtractor 370 subtracts the pre-quantization signal from the quantized signal to produce a cost signal. The updating device 380 updates the coefficients of the feed-forward equalizer 310 and feedback equalizer 362 based on the cost signal and updates coefficients of the post-cursor processing filter 320 based on the cost signal and the white quantized signal.

Because the difference between the input and output of the slicer 340 is small, the behavior of DFE is close to an IIR filter with the transfer function as follows:

$$R(z) = \frac{N(z)}{D(z)} \tag{3}$$

where N(z) is a transfer function of the feed-forward equalizer (FFE) 310, D(z) is a transfer function of the feedback equalizer (FBE) 362.

The decision feedback loop (DFL) can be pipelined by inserting a polynomial

$$Q(z) = \sum_{k=0}^{D_1} q_k z^{-k}, q_0 = 1$$

to the numerator and denominator of equation (3). With the same number of poles and zeros being inserted in the numerator and denominator of equation (3), it is able to de-correlate the dependence of the output and the first D_1 ISI terms. The corresponding equation is given below:

$$R(z) = \frac{N(z)}{D(z)} = \frac{Q(z)N(z)}{Q(z)D(z)} = \frac{Q(z)N(z)}{1 - z^{-D_1} + R(z)} \tag{4}$$

where

$$R(z) = \sum_{k=0}^{D_1} r_k z^{-k}.$$  

With the extra delay device 361 that includes D_1 delay elements, the feedback equalizer 362 on the decision feedback loop (DFL) can be pipelined with D_1 pipeline stages. Then, a highest operating clock rate of the pipeline adaptive decision feedback equalizer 300 can be increased to a factor of (D_1+1).

The coefficients of the feed-forward equalizer (FFE) 310 and feedback equalizer (FBE) 362 are dynamically updated based on minimizing a first cost function: \(\|e(n)\|^2\), where e(n) is the cost signal. That is, the updating device 380 dynamically adjusts the coefficients of the feed-forward equalizer (FFE) 310 and feedback equalizer (FBE) 362 based on minimizing the first cost function: \(\|e(n)\|^2\). By applying the stochastic gradient-based algorithm and technique of Sum-Relaxation, the coefficients of the feed-forward equalizer (FFE) 310 and feedback equalizer (FBE) 362 can be respectively expressed as follows:

$$C(n) = C(n-D_1) + \mu \sum_{k=0}^{D_1} e(n-D_2) - [X(n-D_1 + k)]$$

$$D(n) = D(n-D_1) + \mu \sum_{k=0}^{D_1} e(n-D_2) - [X(n-D_1 + k)]$$

According to the “Principle of Orthogonality”, the coefficients of the post-cursor processing filter (PCF) 320 are updated based on minimizing a second cost function:
where \( e(n) \) is the cost signal, \( a(n) \) is the white quantized signal, and \( P(n) = \{ P_1, P_2, \ldots, P_D \} \) represents the coefficients of the post-cursor processing filter (PCF) 320. The coefficients of the post-cursor processing filter (PCF) 320 are represented as follows:

\[
P(n) = P(n - D_1) + \mu \sum_{i=2}^{D_1+1} q(n - D_1 - i) e(n - D_1 - i).
\]

where \( Z(n) = \{ a(n-1), \ldots, a(n-D_1) \} \).

FIG. 4 shows an embedded circuit of present invention with a speedup factor of three \((D_1 = 2)\). This is, the iteration bound of serial ADFE as shown in FIG. 1 is three times than the PCFADFE 400. This implies that there is two extra delay elements \((D_1 = 2)\) inserted into the delay feedback loop (DFL). It is assumed that the transmitted data, \( w(n) \) (change \( a(n) \) to \( w(n) \)), is an independent sequence, and input data of receiver is \( x(n) \). The input data \( x(n) \) can be expressed as:

\[
x(n) = b_0 + b_1 x(n-1) + b_2 x(n-2),
\]

where \( b_0, b_1, b_2 \) are channel impulse response, \( v(n) \) is the additive white Gaussian noise (AWGN). The number of taps in FFE 310 and FBE 362 are three and two, respectively. Since \( D = \{2\} \), the number of taps in the PCF is three \((D_1 + 1)\) in this embodiment. The 1-th coefficients of FFE 310, PCF 320 and FBE 362 at time instance \( n \) are denoted as \( c_1, p_1 \), and \( b_1 \), respectively. With above notations, an estimation error or cost function \( e(n) \) can be expressed as:

\[
e(n) = w(n) - F(n) - P(n)
\]

\[
= w(n) - F(n) - p_1 F(n - 1) - p_2 F(n - 2) - B(n)
\]

\[
F(n) = \sum_{i=0}^{2} c_i x(n + i),
\]

\[
B(n) = \sum_{i=1}^{2} b_i w(n - 2 - i),
\]

where \( F(n) \) is the output of FFE 310, and \( B(n) \) is the output of FBE 362. \( P(n) \) denotes the total effect of PCF 320 and FBE 310 at time instance \( n \), and can be written as:

\[
P(n) = p_1 F(n - 1) + p_2 F(n - 2) + B(n)
\]

where \( \eta(n) \) is a noise component.

In the serial ADFE 100 as shown in FIG. 1, the objective of the FFE 310 is to minimize \( E[e^2(n)] \). In the FFE 310 of the PCFADFE 400, it intends to minimize \( e^2(n) \) instead of \( E[e^2(n)] \). In order to apply stochastic gradient-based algorithm, it must find the gradient of this cost function \( e(n) \). Moreover, the total effect of PCF 320 and FBE 362 in time instance \( n \) can be considered as a constant. Hence, the gradients corresponding to \( c_i \) are listed as follows:

\[
\frac{\partial e^2(n)}{\partial c_0} = -2e(n)x(n),
\]

\[
\frac{\partial e^2(n)}{\partial c_1} = -2e(n)x(n + 1),
\]

\[
\frac{\partial e^2(n)}{\partial c_2} = -2e(n)x(n + 2),
\]

The results as listed above are similar to those of the serial ADFE 100. Hence, the main functionality of the FFE 310 in PCFADFE 400 is to cancel the precursor ISI terms. In present embodiment, it employs a dedicated PCF 320 to de-correlate the correlation between the first two post-cursor ISI terms and ADFE output. The remaining ISI terms will be canceled by FFE 310 and FBE 362, respectively.

Considering the PCF 320 and FBE 362, the output of FFE 310 at time instance \( n \) can be written as:

\[
F(n) = \sum_{i=0}^{1} c_i x(n + i) = \sum_{i=1}^{2} x_i w(n - i).
\]

\[
F(n) \text{ represents sum of the residual ISI terms that cannot be canceled by FFE 310 at time instance } n. \text{ It is noted that, in the serial ADFE 100 as shown in FIG. 1, the prediction error must be orthogonal to the observations in the steady state, which is known as “Orthogonal Principle” in the literature of adaptive signal processing. It implies that minimizing the estimation error is equivalent to de-correlate the correlation between observations and filter output. Therefore, the objective of the PCF 320 is to minimize the following two expectation terms:}

\[
\text{Min} E[e^2(n)(n - 1)],
\]

\[
\text{Min} E[e^2(n)(n - 2)],
\]

where \( p_1, p_2 \) are the coefficients of the 2-tap PCF 320. Next, the gradients corresponding to these cost functions are listed as follows:

\[
\frac{\partial E^2[w(n - 1)w(n)]}{\partial p_1} = 2p_1 + p_2 w(n - 1),
\]

\[
= -2p_1 E[e(n)(n - 1)] E[w(n)],
\]

\[
\frac{\partial E^2[w(n - 2)w(n - 2)]}{\partial p_2} = 2p_2 + p_2 w(n - 2),
\]

\[
= -2p_2 E[e(n)(n - 2)] E[w(n - 2)].
\]

Because the direction of gradient is more important than the magnitude of gradient in stochastic gradient-based algorithm, it can approximate the gradient of (15) as follows:

\[
\frac{\partial E[w(n - 1)^2(n)]}{\partial p_1} = -2E[e(n)(n - 1)],
\]
The equations derived for this embodiment can be generalized to the general case with arbitrary taps and arbitrary speedup factor. Finally, by combining with Delayed-LMS, Sum Relaxed Look-ahead and generalized cases of (11a), (15a), (16a), the equations to describe the PCTAFDE 400 embodiment can be written as

\[ X(n) = [x(n), ..., x(n-N_F+1)], \]
\[ Y(n) = [\delta(n-D_1-1) ... \delta(n-D_1-N_G)] \]
\[ Z(n) = [\delta(n) ... \delta(n-D_1)], \]
\[ P(n) = [P_1(n) ... P_{2p}(n)], \]
\[ F(n) = C^T(n-D_1)X(n), \]
\[ B(n) = D^T(n-D_1)Y(n), \]
\[ \delta(n) = \sum_{j=\tau} \left( \sum_{i=\tau} p_i \delta(n-D_1 \tau + j) + B(n) \right), \]
\[ c(n) = \delta(n) - \delta(n), \]
\[ C(n) = C(n-D_1) + \mu \sum_{i=\tau} c(n-D_2 - i)X(n-D_2 - i), \]
\[ D(n) = D(n-D_1) + \mu \sum_{i=\tau} c(n-D_2 - i)Y(n-D_2 - i), \]
\[ P(n) = P(n-D_1) + \mu \sum_{i=\tau} c(n-D_2 - i)Z(n-D_2 - i), \]

where \( p_j \) denotes the j-th coefficient of the PCF 320. The corresponding hardware architecture of PCTAFDE 400 is shown in FIG. 4, where \( D_{\mu} \) are the dummy delays in order to pipeline feed-forward part of PCTAFDE 400.

To verify the performance of present invention, a simulation is performed on the serial ADFE 100, PIPEADFE 200 and PCTAFDE 400 according to the present invention. In the simulation, three types of channel models are employed. In the first channel model (Channel I), it assumes that the channel impulse response, \( h=[0.2, 0.6, 1.0, -1.0, -0.6, -0.2] \), is obtained from a Lorentzian pulse mode. The second channel impulse response (Channel II), \( h=[0.3365, 0.3365] \), is obtained from traditional channel models. The third channel impulse response (Channel III) is the typical channel impulse response of UTP-CAI-5, which is often employed in fast Ethernet applications. The transmitted data \( w(n) \) for all channel models is a PAM5 random sequence, \( w(n) \in [-1, -0.5, 0, 0.5, 1] \).

In the first simulation, it evaluate the convergence performance of both equalizers with input SNR = 30 dB. The parameter settings of serial ADFE 100, PIPEADFE 200 and PCTAFDE 400 according to the present invention for these three channel models are listed in FIG. 5. With the parameter setting, the learning curves of PIPEADFE 200 and PCTAFDE 400 for these channel models are shown in FIG. 6. Based on the results shown in FIG. 6, it shows that the convergence rate of PCTAFDE 400 is faster than that of PIPEADFE 200. That is, the convergence performance is significantly improved by introducing the post-cursor processing filter (PCF) 320. It is known that the convergence rate of the conventional LMS-based serial ADFE 100 depends on the step size and the channel characteristics, which relate to the eigenvalue \( \lambda_0 \) of the received signal autocorrelation matrix. If the channel amplitude and phase distortions are small, the eigenvalue ratio \( \frac{\mu}{\lambda_0} \) is close to one and, the serial ADFE 100 converges to its optimal tap coefficients relatively fast. On the contrary, if the channel exhibits poor spectral characteristics, such as relatively large attenuation in a part of its spectrum, the eigenvalue ratio will be larger than one (i.e., \( \frac{\mu}{\lambda_0} \approx \frac{\lambda_1}{\lambda_0} \approx 1 \)). Thus, the convergence rate of LMS-based serial ADFE will be slow. By using the post-cursor processing filter (PCF), the decisions or the training sequences can be applied to the updating mechanism. By applying the train sequences or decisions into the updating mechanisms, the eigenvalue spread of input signal should be reduced. Thus, the convergence rate of PCTAFDE can be faster than the PIPEADFE 200.

As shown in FIG. 6, it is known that the PIPEADFE 200 and the PCTAFDE 400 suffer from output SNR degradation in comparison with the serial ADFE 100. FIG. 7 shows how the output SNR of PIPEADFE 200 and PCTAFDE 400 is degraded as the speedup factor is increased. The channel model used and the parameters of PIPEADFE 200 and PCTAFDE 400 are the same as shown in FIG. 5, except that \( D_{\mu} \), the speedup=1 and input SNR=28.451. The number of transmitted data samples in both PIPEADFE 200 and PCTAFDE 400 is 10000. As shown, the output SNR and speedup factor are the x and y coordinates respectively. It can be seen that both PIPEADFE 200 and PCTAFDE 400 have an output SNR loss of about 0.5 dB per unit increase in the speedup factor. Because the output SNR depends on the number of taps in FFE and PCF, it can choose the number of taps in FFE and PCF in order to make both architectures achieve the same output SNR, wherein the number of taps of FFE in PIPEADFE 200 is \( N_\mu D_\mu \), the number of taps of FFE in PCTAFDE 400 is \( N_F \). The number of taps of PCF in PCTAFDE 400 is \( D_1 \). Moreover, the number of taps in FFE is fixed on \( N_F \). (Note that \( N_\mu \) and \( N_F \) are the number of taps of FFE and FBE in serial ADFE 100). The speedup factor versus hardware complexity is shown in FIG. 8. It can be seen that the hardware complexities of PIPEADFE 200 and PCTAFDE 400 are the same. Nevertheless, the convergent rate of PCTAFDE 500 is much faster than that of the PIPEADFE 200.

In view of the foregoing, it is known that the present invention utilizes the post-cursor processing filter (PCF) to not only increase the operating clock rate with arbitrary speedup factor but also dramatically improve the convergence rate of the overall system. Furthermore, the hardware overhead of the present invention is the same as the pipeline ADFE 200 (PIPEADFE).

Although the present invention has been explained in relation to its preferred embodiment, it is to be understood that many other possible modifications and variations can be made without departing from the spirit and scope of the invention as hereinafter claimed.
What is claimed is:

1. A fast convergent pipelined adaptive decision feedback equalizer using a post-cursor processing filter, comprising:
   a feed-forward equalizer for receiving input samples and eliminating pre-cursor of the input samples;
   a post-cursor processing filter coupled to the feed-forward equalizer and producing an output signal;
   an adder for adding the output signal of the post-cursor processing filter and a feedback signal to producing an pre-quantization signal;
   a slicer coupled to the adder for quantizing the pre-quantization signal and producing a white quantized signal;
   a register coupled to the slicer for holding the white quantized signal;
   a pipelined feedback equalizer having plurality of pipeline stages and coupling to the register for eliminating the post-cursor of the white quantized signal and producing the feedback signal;
   a subtractor for subtracting the pre-quantization signal from the quantized signal to produce a cost signal; and
   an updating device for updating coefficients of the feed-forward equalizer and pipelined feedback equalizer based on the cost signal and updating coefficients of the post-cursor processing filter based on the cost signal and the white quantized signal.

2. The fast convergent pipelined adaptive decision feedback equalizer as claimed in claim 1, wherein the pipelined feedback equalizer comprises a delay device coupled to the register for delaying the white quantized signal, and a feedback equalizer coupled to the delay device for eliminating the post-cursor of the white quantized signal and producing the feedback signal.

3. The fast convergent pipelined adaptive decision feedback equalizer as claimed in claim 2, wherein the post-cursor processing filter is formed by inserting the same poles and zeros pairs:

   \[ P(z) = \frac{N(z)}{D(z)} = \frac{Q(z)N(z)}{Q(z)D(z)} \frac{Q(z)N(z)}{1 - z^{-D_1}R(z)} \]

   where \( N(z) \) is a transfer function of the feed-forward equalizer, \( D(z) \) is a transfer function of the feedback equalizer,

   \[ Q(z) = \sum_{i=0}^{D_1} a_i z^{-i} \]

   is a transfer function of the post-cursor processing filter, \( D_1 \) is the number of delay elements in the delay device.

4. The fast convergent pipelined adaptive decision feedback equalizer as claimed in claim 3, wherein a highest operating clock rate of the pipeline adaptive decision feedback equalizer can be increased to a factor of \((D_1+1)\).

5. The fast convergent pipelined adaptive decision feedback equalizer as claimed in claim 1, wherein the coefficients of the feed-forward equalizer and feedback equalizer are updated based on minimizing a first cost function:

   \[ \min E[c(n)+\alpha(n-1)], \min E[c(n)+\alpha(n-2)], \ldots \]

   \[ \min E[c(n)+\alpha(n-D_1)] \]

where \( c(n) \) is the cost signal, \( \alpha(n) \) is the white quantized signal, and

\( P(n) = [P_1, P_2, \ldots, P_D] \) represents the coefficients of the post-cursor processing filter.

6. The fast convergent pipelined adaptive decision feedback equalizer as claimed in claim 1, wherein the coefficients of the post-cursor processing filter are updated based on minimizing a second cost function:

   \[ \min E[c(n)+\alpha(n-1)], \min E[c(n)+\alpha(n-2)], \ldots \]

   \[ \min E[c(n)+\alpha(n-D_1)] \]

where \( c(n) \) is the cost signal, \( \alpha(n) \) is the white quantized signal, and \( P(n) = [P_1, P_2, \ldots, P_D] \) represents the coefficients of the post-cursor processing filter.

7. The fast convergent pipelined adaptive decision feedback equalizer as claimed in claim 5, wherein the coefficients of the post-cursor processing filter are updated based on minimizing a second cost function:

8. The fast convergent pipelined adaptive decision feedback equalizer as claimed in claim 7, wherein the coefficients of the post-cursor processing filter are:

   \[ P(n) = P(n-D_1) + \alpha \sum_{i=0}^{D-1} \alpha(n-D_1-i)Z(n-D_1-i) \]

   \[ Z(n) = [a(n-1) \ldots a(n-D_1)] \]

   \[ * * * * * \]