Chapter 2
CMOS Processing/Layout Supplement (III)

*Layout of Basic gate:  \textit{NOR2 Gate}
* **NAND2 Gate**

![NAND2 Gate Diagram]

* **Complex Gate:** 
  \[ F = D + A \cdot (B + C) = D + (A \cdot (B + C)) \]

![Complex Gate Diagram]

(c) complete gate
* Layout of Complex CMOS Logic Gates

\[ F = A \cdot (D + E) + (B \cdot C) \]

- How to arrange inputs \( A,B,C,D,E \) so that only one strip of p-diffusion & n-diffusion are used?
- Use Graph theory
• Layout of Complex CMOS Logic Gates (use Arbitrary input order)

• Stick diagram layout of the complex CMOS gate. Order = A, E, B, D, C

\[ F = A \cdot (D + E) + (B \cdot C) \]

Apply Euler path, find a common Euler path for both graphs. The Euler path is defined as an uninterrupted path that traverses each edge (branch) of the graph exactly once. In both cases, the Euler path starts at (x) and ends at (y).

Order = E, D, A, B, C
**Layout of Complex Gate: Case (B)**

\[ Z = A + B + (C \cdot D) \]

**Apply Euler Path**

1. Find Euler paths that cover the graph
2. Find a P-NET and n-NET Euler path that have identical labeling
3. If the path in step 2 are not found, then break the gate in the minimum number of places to achieve step 2 by separate Euler paths.
Another Design example  (CASE C)

- The Boolean function realized by this circuit is  \( Z = (A + D + E) \cdot (B \cdot C) \)
- The input sequence is  \( D, E, A, B, C \)
* Layout of CMOS XNOR Gate

**Case (B)**

\[ Z = A \oplus B = A \cdot B + \overline{A} \cdot \overline{B} = (A + B) \cdot (A \cdot \overline{B}) \]

\[ K = A \cdot B \quad \rightarrow \quad Z = K \cdot (A + B) \]
*Automatic approach to CMOS gate layout

*Function

\[ B = A \cdot C \cdot E = (D + E) \cdot C \cdot E \]

Steps:
(a) Route Vdd, Vss, Gate, output
(b) Order gates and outputs
(c) Rearrange vertical Strips

(a) Route Power, Ground, Gate and Output Signals

(b) Order Gate and Outputs to optimize horizontal transistor connectivity

(c) Rearrange vertical strip ordering to optimize power routing internal gate connections
*Sea-of-gates Layout

- Pre-layout n-diffusion, p-diffusion, Contact cuts, Metal1 (connected to Vdd and Vss)
- Programmed part: Metal-1 (M1), Metal-2 (M2), VIA and VIA2.

Example(a): 3-input NAND gate (NAND3)
Example(b): Two inverters driving a NOR2 gate
**CMOS Standard Cell Design**

- Height is the same
- Width is varied for different cells
- For most standard gates (low-power cell, high-speed cells)

Left: A typical CMOS standard cell mask layout.

Right: (a)(b)(c)(d) Different layouts for NAND3
Standard Cell Layout
(generated by auto
Place-and-Route CAD
tools)
* Gate Array Layout

- Well, diffusion, poly-silicon layers are fixed
- Contact, Metal1, Via, Metal 2 are programmable

*How to make a dense layout?

1. Better use of routing layers—routes can occur over cells.
2. Use of optimum device sizes —the use of smaller devices leads to smaller layouts.
3. Speed and Power Consumption would be the key.
*Layout Style and Capacitance*

FIGURE 5.20 Optimization of CMOS gate layout involving multiple source-drain connections.

with a metal strap or a combination of metal and polysilicon straps where metal routing transparency is required. When considering a transmission gate, the source and drain terminals of the p- and n-transistors are paralleled. According to the layout strategy presented, the layouts shown in Fig. 5.21 would be suitable. Note that in Fig. 5.21(a), no metal lines can pass from left to right. The layout shown in Fig. 5.21(b) is longer but has horizontal metal transparency. The decision on which layout is more suitable would depend on the circuit being designed. For instance, in a shift-register-delay line, Fig. 5.21(a) might be preferred due to its small size. In a data path, where bus lines may have to pass horizontally, Fig. 5.21(b) would be preferred. Figure 5.21(c) shows a metal2 version.