Introduction of Xilinx System Generator on Simulink

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Outline

- Introduction to Simulink System and Generator
- Introduction to Design Flow
- Installation and Setup of Design Tools
  - Software and hardware requirements
  - Installation of Xilinx ISE
  - Setup System Generator
- Lab: Single delay unit (D-Filpflop)
Introduction to Simulink and System generator

- **Simulink**
  - Developed by Mathworks Inc.
  - A Model-based design environment integrated with Matlab
  - Provides various sets of block libraries to help you create, simulate, and test a complicated system, including control system, communication, image processing, etc.

- **System Generator**
  - Developed by Xilinx Corp.
  - Provides device-optimized DSP block library for Simulink
  - Let you model DSP algorithm, generate HDL code, and verify FPGA designs for Xilinx devices in an intuitive and efficient way.
Introduction to Simulink and System generator

- Simulink

- System Generator
Introduction to Design Flow

- Goal: Use Xilinx System Generator to design a DSP system
Installation and Setup of Design Tools

- Software and hardware requirements
  - Windows XP 32-bit edition (recommended)
    (System Generator 10.1 may not support other operating system, like Vista, Win7 64bit-edition)
  - 10GB hard disk space
  - Matlab R2007a, with Simulink 6.6 or higher version
Installation and setup of design tools

- Installation of Xilinx 10.1
- Enter serial number
Installation and setup of design tools

- Installation of Xilinx 10.1
- Note: If DSP Tools option is not selectable, it means System generator does not support your operating system
Installation and setup of design tools

- After finishing installation, go to “start->all programs then find out and launch “project navigator”
Installation and setup of design tools

- Remember to upgrade ISE from ver 10.1 to ver 10.3
  - Help->XilinxUpdate
Installation and setup of design tools

- Setup System Generator
Installation and setup of design tools

- Setup System Generator
  - Choose your matlab installation and click “OK”
Lab

- Introduction : Unit delay
Lab

- Open Matlab
- Click on Simulink button
Lab

- **Simulink environment**

1. Click to open new model
2. Find Xilinx blockset

3. Double click on “Basic Element”
Right click on the Delay element, and then choose "Add to..." option.
Lab

- Repeat previous step to find and add "Gateway In, Gateway Out, Constant, Scope, System Generator" block to your design model.

- You may use “search toolbar” to find blocks.
Lab

❖ Connect model block
  ❖ 1. Click on the source block
  ❖ 2. Press “ctrl” on the keyboard (don’t release) and click on the destination block
Lab

- Connect whole system block
Lab

- Double click on “Gateway In” to setup block parameter
Lab

- Click on “START” to simulate system
Lab

- Double click on “Scope” block to view simulation result
Reference

System Generator for DSP-Getting Started Guide