Introduction to FPGA

Presenter: CMH
Advisor: Prof. An-Yeu Wu
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Outline

- Basic Concepts of FPGA
- Architecture and Feature of Xilinx FPGA
- Reference
Basic Concepts of FPGA
Electronic Components

Source: Dataquest

Logic

Standard Logic

Programmable Logic Devices (PLDs)

SPLDs (PALs)

ASIC

Gate Arrays

Cell-Based ICs

Full Custom ICs

Common Resources

Configurable Logic Blocks (CLB)

- Memory Look-Up Table
- AND-OR planes
- Simple gates

Input / Output Blocks (IOB)

- Bidirectional, latches, inverters, pullup/pulldowns

Interconnect or Routing

- Local, internal feedback, and global

Acronyms

SPLD = Simple Prog. Logic Device
PAL = Prog. Array of Logic
CPLD = Complex PLD
FPGA = Field Prog. Gate Array

Application-Specific IC
Programmable Logic Device

- CPLDs and FPGAs

<table>
<thead>
<tr>
<th>Complex Programmable Logic Device (CPLD)</th>
<th>Field-Programmable Gate Array (FPGA)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Architecture</strong></td>
<td>Gate array-like</td>
</tr>
<tr>
<td>PAL/22V10-like</td>
<td>More Registers + RAM</td>
</tr>
<tr>
<td>More Combinational</td>
<td></td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>Medium-to-high</td>
</tr>
<tr>
<td>Low-to-medium</td>
<td>1K to 3.2M system gates</td>
</tr>
<tr>
<td>0.5-10K logic gates</td>
<td></td>
</tr>
<tr>
<td><strong>Performance</strong></td>
<td>Application dependent</td>
</tr>
<tr>
<td>Predictable timing</td>
<td>Up to 200 MHz today</td>
</tr>
<tr>
<td>Up to 250 MHz today</td>
<td></td>
</tr>
<tr>
<td><strong>Interconnect</strong></td>
<td>Incremental</td>
</tr>
<tr>
<td>“Crossbar Switch”</td>
<td></td>
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</tbody>
</table>
Basic FPGA Architecture

Clocking
- CLIN
- CLK0
- CLK90
- CLKFX

Logic
- Logic gates
- CE
- I1
- I2
- I3
- I4
- O

Memory
- DIA
- DOA
- DIPA
- DOPA
- ADDRA
- CLKA
- DIB
- DOE
- DIPB
- DOPB
- ADDRB
- CLKB

IO Blocks
- Input
- Reg
- DDR mux
- 3-State
- Output
- Reg
- DDR mux
- PAD

Source: Avnet
Basic process technology types of FPGA

- One-time programmable
  - Fuses (destroy internal links with current, bipolar)
  - Anti-fuses (grow internal links, CMOS)
  - PROM (Read-Only Memory technology)

- Re-programmable
  - EPROM (Erasable Programmable Read-Only Memory technology)
  - EEPROM
  - Flash
  - SRAM
FPGA vs. ASIC Design Flow Comparison

Source: Xilinx
## Comparison

<table>
<thead>
<tr>
<th></th>
<th>Full-Custom ICs</th>
<th>Cell-Based ICs</th>
<th>Gate Arrays</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>●●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Integration Density</td>
<td>●●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>High-Volume Device Cost</td>
<td>●●</td>
<td>●●</td>
<td>●</td>
<td>●</td>
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<tr>
<td>Low-Volume device Cost</td>
<td></td>
<td></td>
<td>●</td>
<td>●●</td>
</tr>
<tr>
<td>Time to Market</td>
<td></td>
<td></td>
<td>●</td>
<td>●●</td>
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<tr>
<td>Risk Reduction</td>
<td>●●</td>
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<td>●</td>
<td>●●</td>
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<tr>
<td>Future Modification</td>
<td></td>
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<td>●●</td>
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<tr>
<td>Development Tool</td>
<td>●</td>
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<td>●●</td>
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<tr>
<td>Educational Purpose</td>
<td>●●</td>
<td></td>
<td>●</td>
<td>●●</td>
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</tbody>
</table>
# FPGA & ASIC Design Advantages

<table>
<thead>
<tr>
<th>FPGA Design Advantages</th>
<th>ASIC Design Advantages</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Faster time-to-market</strong> - no layout, masks or other manufacturing steps are needed</td>
<td><strong>Full custom capability</strong> - for design since device is manufactured to design specs</td>
</tr>
<tr>
<td><strong>No upfront NRE</strong> (non recurring expenses) - costs typically associated with an ASIC design</td>
<td><strong>Lower unit costs</strong> - for very high volume designs</td>
</tr>
<tr>
<td><strong>Simpler design cycle</strong> - due to software that handles much of the routing, placement, and timing</td>
<td><strong>Smaller form factor</strong> - since device is manufactured to design specs</td>
</tr>
<tr>
<td><strong>More predictable project cycle</strong> - due to elimination of potential re-spins, wafer capacities, etc.</td>
<td><strong>Higher raw internal clock speeds</strong></td>
</tr>
<tr>
<td><strong>Field reprogramability</strong> - a new bitstream can be uploaded remotely</td>
<td><strong>Low power</strong></td>
</tr>
</tbody>
</table>

Source: Xilinx
Major Vendors

SRAM-based FPGAs
- Xilinx, Inc.
- Altera Corp.
- Atmel
- Lattice Semiconductor

Flash & antifuse FPGAs
- Actel Corp.
- Quick Logic Corp.

control over 80% of the market
Xilinx Product Line

Xilinx Products

- IP
- EasyPath
- Device
- Solution
- Tool

- CPLD
  - CoolRunner
  - CoolRunner-II

- FPGA
  - Spartan
  - Virtex

- ISE

Xilinx Products

pp. 12
Full Xilinx Design Support

<table>
<thead>
<tr>
<th>CPLD</th>
<th>Low-cost FPGA</th>
<th>High-performance FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC9500</td>
<td>SPARTAN-3</td>
<td>VIRTEX V4</td>
</tr>
<tr>
<td>XC9500XL</td>
<td>SPARTAN-3E</td>
<td>VIRTEX V5</td>
</tr>
<tr>
<td>CoolRunner-II</td>
<td>SPARTAN-3A</td>
<td></td>
</tr>
</tbody>
</table>

Higher Device density and Performance
Architecture and Feature of Xilinx FPGA
Overview

- All Xilinx FPGAs contain the same basic resources
  - Slices grouped into Configurable Logic Blocks (CLBs)
    - Contain combinatorial logic and register resources
  - IOBs
    - Interface between the FPGA and the outside world
  - Programmable interconnect
  - Other resources
    - Memory
    - Multipliers
    - Global clock buffers
    - Boundary scan logic

Source: Avnet
Virtex-II Architecture

First family with Embedded Multipliers to enable high-performance DSP

- I/O Blocks (IOBs)
- Configurable Logic Blocks (CLBs)
- Clock Management (DCMs, BUFGMUXes)
- Block SelectRAM™ resource
- Embedded multipliers
- Programmable interconnect

XILINX®

VIRTEX-II PRO

XC2VP70™
FF1517CGB0517
D1354894A
Taiwan

ACCESS IC LAB
Graduate Institute of Electronics Engineering, NTU
CLBs and Slices

Combinational and sequential logic implemented here

- Each Virtex™-II CLB contains four slices
  - Local routing provides feedback between slices in the same CLB, and it provides routing to neighboring CLBs
  - A switch matrix provides access to general routing resources
Slice Resources

- Each slice contains two:
  - Four inputs lookup tables
  - 16-bit distributed SelectRAM
  - 16-bit shift register

- Each register:
  - D flip-flop
  - Latch

- Dedicated logic:
  - Muxes
  - Arithmetic logic
    - MULT_AND
    - Carry Chain
Look-Up Tables

- Combinatorial logic is stored in Look-Up Tables (LUTs)
  - Also called Function Generators (FGs)
  - Capacity is limited by the number of inputs, not by the complexity
- Delay through the LUT is constant

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>Z</th>
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<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
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<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Distributed RAM

- LUTs used as memory inside the fabric
- Flexible, can be used as RAM, ROM, or shift register
- Distributed memory with fast access time
- Cascadable with built-in CLB routing
- Applications
  - Linear feedback shift register
  - Distributed arithmetic
  - Time-shared registers
  - Small FIFO
  - Digital delay lines ($Z^{-1}$)
The SRL16E

- The 16 SRAM cells have been organized into a shift register
  - The ‘CE’ is used, in conjunction with the clock, to write data into the first flip-flop and for all other data to move right by one position
  - Because this is a predictable operation, no address is required for writing

- The SRL16E is excellent in implementing efficient DSP Functions
  - A very efficient way to delay data samples
  - Shifting samples and scanning at faster rate
System Memory

- System Memory – Distributed RAM, Block RAM and External Memory

Distributed Memory
- Cascadable LUT-based Memory
- Single- or dual-port
- RAM / ROM / Shift-Reg modes
- Up to 122,880 16-b Memory/chip

Block RAM / ROM
- 18Kbits/block
- True Dual-Port™
- Asymmetric Width
- x1 to x36
- Supports Parity
- Up to 3.5Mb / chip

User Benefits
- Fast & efficient logic
  - Digital delay lines
  - LFSR counters
  - Table look-up
- Highest flexibility
  - M-bit to N-bit translate
  - ROM-based FSM
  - Boot code storage

DDR/QDR Interface
- External RAM/CAM
- Dedicated DDR registers
- 300+ Mbps
Clock Management

- System clock management - DLLs
  - Clock Mirror
  - Multiplication
    - 1 DLL for 2x
    - Combine 2 DLL for 4x
  - Division
    - Selectable division values - 1.5, 2, 2.5, 3, 4, 5, 8, or 16
  - Phase Shift
    - 0, 90, 180, 270
Clock Management

- System clock management – DCMs

**DLL: Used to de-skew clocks**
- 50 percent duty-cycle correction
- Phase shifting
- Clock multiplication and division

**DFS: Used to create derived clocks**
- $CLKFX$ is any $M/D$ product of $CLKIN$ frequency
  - $M = 2$ to $32$, $D = 1$ to $32$
Embedded multiplexer

- 18-bit x 18-bit 2’s Complement Signed Multiplier
  - 18 x 18 bit Signed or 17 x 17 bit Unsigned operation
  - Fast connection to the adjacent 18Kb block RAM
  - Optimized for Low Power / High Performance

<table>
<thead>
<tr>
<th>Device</th>
<th>Multipliers</th>
<th>BRAM (Kbits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC2V40</td>
<td>4</td>
<td>72</td>
</tr>
<tr>
<td>XC2V80</td>
<td>8</td>
<td>144</td>
</tr>
<tr>
<td>XC2V250</td>
<td>24</td>
<td>432</td>
</tr>
<tr>
<td>XC2V500</td>
<td>32</td>
<td>576</td>
</tr>
<tr>
<td>XC2V1000</td>
<td>40</td>
<td>720</td>
</tr>
<tr>
<td>XC2V1500</td>
<td>48</td>
<td>864</td>
</tr>
<tr>
<td>XC2V2000</td>
<td>56</td>
<td>1,008</td>
</tr>
<tr>
<td>XC2V3000</td>
<td>96</td>
<td>1,728</td>
</tr>
<tr>
<td>XC2V4000</td>
<td>120</td>
<td>2,160</td>
</tr>
<tr>
<td>XC2V6000</td>
<td>144</td>
<td>2,592</td>
</tr>
<tr>
<td>XC2V8000</td>
<td>168</td>
<td>3,024</td>
</tr>
<tr>
<td>XC2V10000</td>
<td>192</td>
<td>3,456</td>
</tr>
</tbody>
</table>
Enabling high-performance DSP

Virtex-II introduced the embedded 18x18 multiplier

- Situated between the Block RAMs and CLB array to enable high-performance multiply-accumulate operations
- This dramatically increased multiplier speed and density compared to LUT based multipliers and enabled FPGA based DSP
Virtex-4 Features

- 200,000 Logic Cells
- 500 MHz Xesium™ Differential Clocking
- 6.5 Gbps RocketIO™ Transceivers
- PowerPC® Processor with APU
- AES Secure Chip Design Security
- 1 Gbps SelectIO™ with ChipSync™
- 10/100/1000 Ethernet MAC
- BRAM with FIFO & ECC
- XtremeDSP™ Slice
Virtex-5 Common Features

- 30% Higher Performance
- New Capability
- Advanced Configuration Options
- 6-LUT + Express Fabric
- 36Kb Dual-Port Block RAM / FIFO with ECC
- Higher Bandwidth
- SelectIO with IDELAY/ODELAY and SerDes
- 10/100/1000 Mbps Ethernet MAC
- PCI-Express Endpoint Blocks
- GTP 3.75 Gbps Transceivers
- GTX 6.5 Gbps Transceivers
- PowerPC440 Processors
- 25x18 DSP Slices
- 550 MHz Clock Management
- Integrated System Monitor A/D Converter

Higher Precision
Precision + low jitter
Saves Logic

pp. 28
Advanced Logic Structure

- True 6-input LUTs
- Exclusive 64-bit distributed RAM option per LUT
- Exclusive 32-bit or 16-bit x 2 shift register
DSP48 Block

Includes a high performance arithmetic unit and a multiplier
DSP48 Block

Dynamically Programmable DSP Op Modes

- Enables time-division multiplexing for DSP
- Over 40 different modes
- Each XtremeDSP Slice individually controllable
- Change operation in a single clock cycle
- Control functionality from logic, memory or processor

<table>
<thead>
<tr>
<th>OpMode</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero</td>
<td>+/- Cin</td>
</tr>
<tr>
<td>Hold P</td>
<td>+/- (P + Cin)</td>
</tr>
<tr>
<td>A:B Select</td>
<td>+/- (A:B + Cin)</td>
</tr>
<tr>
<td>Multiply</td>
<td>+/- (A * B + Cin)</td>
</tr>
<tr>
<td>C Select</td>
<td>+/- (C + Cin)</td>
</tr>
<tr>
<td>Feedback Add</td>
<td>+/- (C + P + Cin)</td>
</tr>
<tr>
<td>36-Bit Adder</td>
<td>+/- (A:B + C + Cin)</td>
</tr>
<tr>
<td>P Cascade Select</td>
<td>PCIN +/- Cin</td>
</tr>
<tr>
<td>P Cascade Feedback Add</td>
<td>PCIN +/- (P + Cin)</td>
</tr>
<tr>
<td>P Cascade Add</td>
<td>PCIN +/- (A:B + Cin)</td>
</tr>
<tr>
<td>P Cascade Multiply Add</td>
<td>PCIN +/- (A * B + Cin)</td>
</tr>
<tr>
<td>P Cascade Add</td>
<td>PCIN +/- (C + Cin)</td>
</tr>
<tr>
<td>P Cascade Feedback Add</td>
<td>PCIN +/- (C + P + Cin)</td>
</tr>
<tr>
<td>P Cascade Add Add</td>
<td>PCIN +/- (A:B + C + Cin)</td>
</tr>
<tr>
<td>Hold P</td>
<td>PCIN +/- Cin</td>
</tr>
<tr>
<td>Double Feedback Add</td>
<td>+/- (P + Cin)</td>
</tr>
<tr>
<td>Feedback Add</td>
<td>+/- (A:B + Cin)</td>
</tr>
<tr>
<td>Multiply-Accumulate</td>
<td>+/- (A * B + Cin)</td>
</tr>
<tr>
<td>Feedback Add</td>
<td>+/- (C + Cin)</td>
</tr>
<tr>
<td>Double Feedback Add</td>
<td>+/- (C + P + Cin)</td>
</tr>
<tr>
<td>Feedback Add Add</td>
<td>+/- (A:B + C + Cin)</td>
</tr>
<tr>
<td>C Select</td>
<td>+/- Cin</td>
</tr>
<tr>
<td>Feedback Add</td>
<td>+/- (P + Cin)</td>
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<tr>
<td>36-Bit Adder</td>
<td>+/- (A:B + Cin)</td>
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<tr>
<td>Multiply-Add</td>
<td>+/- (A * B + Cin)</td>
</tr>
<tr>
<td>Double</td>
<td>+/- (C + Cin)</td>
</tr>
<tr>
<td>Double Add Feedback Add</td>
<td>+/- (C + P + Cin)</td>
</tr>
<tr>
<td>Double Add</td>
<td>+/- (A:B + C + Cin)</td>
</tr>
</tbody>
</table>
DSP48 Block

Useful For More Than DSP

- **6:1 high-speed, 36-bit Multiplexer**
  - Use four XtremeDSP Slice and op-modes
  - 500 MHz performance using no programmable logic
    - Save 1584 LCs to build equivalent function in logic

- **Dynamic 18-bit Barrel Shifter**
  - Use two XtremeDSP slices
  - Use dedicated cascade routing and integrated 17-bit shift
    - Save 1449 LCs to build equivalent function in logic

- **36-bit Loadable Counter**
  - Use a single XtremeDSP slice, achieve 500 MHz performance
    - Save 540 LCs to build equivalent function in logic
DSP48E Block

Includes a high performance ALU, pattern compare, and a multiplier

450 MHz operation in the slowest speed grade
DSP48E

- Virtex-5SX introduced a few new improvements in the DSP48E “enhanced” DSP block

- The adder block was modified to become a multifunctional ALU. A pattern compare was added to support the detection of saturation, overflow and underflow conditions

- A 48-bit carry chain supports the propagation of partial sum and product carry’s so multiple DSP48E blocks can be chained to give higher bit precision

- ALU opcodes are dynamically controlled allowing functional changes on a clock cycle basis
Clock Management Technology

- The Clock Management Tiles (CMTs) in the Virtex-5 family provide very flexible, high performance clocking.

- Each CMT contains two DCMs and one PLL
  - You may utilize them to generate clock for your design
Reference

For more details, visit


Virtex-5 FPGA User Guide