Example: CMOS Inverter Layout

In this tutorial, a simple CMOS inverter layout will be drawn step by step. We will start with a simple design idea and will complete the mask layout using different techniques.

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1. Design Idea

To draw the mask layout of a circuit, two main items are necessary at the beginning:

1. A circuit schematic
2. A signal flow diagram

1. Circuit schematic

Any physical layout will actually correspond to a circuit schematic. It is important that the schematic of a functionally correct circuit is present and the layout is drawn according to the schematic (and not the other way around).

The schematic will then contain exact connection diagram and individual device properties. Two example inverter schematics can be seen below. While both schematics are identical, the one on the right is drawn in a way to resemble the final layout.

In this example the NMOS transistor and the PMOS transistor have identical dimensions W=1.2u and L=0.6u

2. Signal flow diagram

A layout can be drawn in a number of different ways. The most important factor
determining the actual layout is the signal flow. The layout will almost in all cases be a part of a larger structure or the basic building element of an array of identical blocks.

In modern fabrication technologies, more than one physical layer can be used to transfer signals. For example with the fabrication technology used throughout this manual, a total of 4 layers (poly, Metal-1, Metal-2, Metal-3) can be used. The general flow of the signal connections as well as their layers needs to be pre-determined. The following is an sample flow diagram used for the example layout:

![Flow Diagram](image)

In this flow diagram, it has been decided that all signals are on the same layer (blue, Metal-1) and that all signals will travel horizontally. Note that the signal flow diagram is just a concept that you can visualize for a particular circuit, or a simple scratch that you can scribble on the back of an envelope. The actual mask layout will *roughly* follow this concept.
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2. Create Layout Cellview

We will assume, that you have logged on and started Cadence Design Tools, and that you already have created a design library for yourself. Please refer to Starting Cadence Section if you have not done so.

1. From the Library Manager, choose File then New and then Cellview
   (File --> New --> Cellview)

2. Enter cellname and choose layout cellview

A dialog box will appear prompting you for the design library, cellname and cellview. Make sure that the library name corresponds to your design library, choose a name for your cell and choose Virtuoso as the design tool. The cellview will be selected as layout.
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3. Virtuoso and LSW

Two design windows will pop-up after you have entered the design name.

LSW

The Layer Selection Window (LSW), lets the user select different layers of the mask layout. Virtuoso will always use the layer selected in the LSW for editing. The LSW can also be used to determine which layers will be visible and which layers will be selectable. To select a layer, simply click on the desired layer within the LSW.

Virtuoso

Virtuoso is the main layout editor of Cadence design tools. There is a small button bar on the left side of the editor. Commonly used functions can be accessed through pressing these buttons. There is an information line at the top of the window. This information line, (from left to right) contains the X and Y coordinates of the cursor, number of selected objects, the traveled distance in X and Y, the total distance and the command currently in use. This information can be very handy while editing. At the bottom of the window, another line shows what function the mouse buttons have at any given moment. Note that these functions will change according to the command you are currently executing.
Most of the commands in Virtuoso will start a mode, the default mode is selection, as long as you do not choose a new mode you will remain in that mode. To quit from any mode and return to the default selection mode, the "ESC" key can be used.
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4. Drawing the N-Diffusion (Active)

Now we will start drawing our first transistor, which will be the NMOS transistor of the CMOS inverter. From the schematic, we know that this transistor has a channel width of 1.2u. The width of the transistor will correspond to the width of the active area. We will select the n-diffusion layer and draw a rectangular active area to define the transistor.

1. Select nactive layer from the LSW

2. From the Create menu in Virtuoso select Rectangle

( Create --> Rectangle )

3. Draw the box

You are now in rectangle mode. Select the first corner of rectangle in the layout window (you may select any point within the window but try to select a point close to the origin), click once, and then move the mouse cursor to the opposite corner. Using the information bar, draw a box that is 3.6u horizontal and 1.2u vertical. All units are in micrometers by default. To simplify the drawing, a grid of half a lambda is used, that is the cursor moves in 0.15u increments only.
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5. The Gate Poly

The second step is to draw the gate. We will use a vertical polysilicon rectangle to create the channel. Note that the length of the transistor channel will be determined by the width of this poly rectangle.

1. Select poly layer from the LSW

2. From the menu Misc choose Ruler
   ( Misc --> Ruler )

The ruler is a very handy function. In our case we need to draw the poly rectangle in the middle of the diffusion region. Furthermore, design rules tell us that poly must extend at least by 0.6u (2 Lambda) from edge of the diffusion. To pinpoint the location of the poly gate we can use two rulers. One ruler will be used to determine the horizontal distance of the poly gate from the diffusion edge, while a second ruler will show the minimum amount of poly extension outside the diffusion according to the design rules.

3. Draw poly rectangle
The starting point is pinpointed by two rulers. The rectangle function is used to draw a poly rectangle that is 0.6u horizontal and 2.4u vertical.
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6. Making Active Contacts

The next step is to make the active contacts. These contacts will provide access to the drain and source regions of the NMOS transistor.

1. Select the *ca* (Active Contact) layer from the LSW.

2. Use the ruler to pinpoint a location **0.30u from the edges of diffusion**.

3. Create a square with a **width and height of 0.6u** within the active area.

4. From the Edit menu choose *Copy*  
   ( Edit --> Copy )
You could choose to draw the second contact the same way as you have drawn the first one. However, copying existing features is also a viable alternative.

The copy dialog box will pop-up as soon as you select the copying mode. For this operation the default values are appropriate. The *Snap Mode* is an interesting option. When this is in *orthogonal* setting the copied objects will move only along one axis. This is a good feature to help you avoid alignment problems.

![Copy dialog box](image)

5. Copy the contact

After you enter the copy mode, an object must be selected. Click in the contact, you'll notice that the outline of contact will attach to your cursor. Now move the object, and click when you are satisfied with the location.

![Copy mode](image)

*Design rules* state that the minimum contact to poly spacing must be 0.6u (2 lambda). You can use a ruler to pinpoint the location. Please note that you can interrupt any mode for placing a ruler (and zooming in and out). After you are finished (by hitting "ESC" key) you'll return to the mode you were in.
Now you have placed an active contact each into the source and drain diffusion regions of the transistor.
Active contacts in fact only define holes in the oxide (connection terminals). The actual connection to the corresponding diffusion region is made of the Metal layer.

1. Select layer *Metal-1* from the LSW

2. Draw two rectangles 1.2u wide to cover the contacts

Note that *Metal-1* has to extend over the contact in all directions by at least 0.3u (1 lambda).
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8. The N-Select Layer

Each diffusion area of each transistor must be selected as being of n-type or p-type. This is accomplished by defining the "window" of n-type (or p-type) doping (implantation), through a special mask layer called n-select (p-select).

1. Select \texttt{nselect} layer from the LSW.

2. Draw a rectangle \textit{extending over the active area by 0.6\textmu m (2 lambda)} in all directions.

This is it! Our first transistor is finished, Now let us make a few million more of the same :-)

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9. Drawing the P-Diffusion (Active)

Now that we have drawn the NMOS transistor, the next step is to draw the PMOS transistor. The basic steps involved in drawing the PMOS are the same.

1. Select \textit{pactive} layer from the LSW

2. Draw a rectangle 3.6\textmu m by 1.2\textmu m

You can use the cursor keys and the zoom function to find yourself a place to build the transistor. Make sure you leave enough separation between the NMOS and the PMOS. Note that the PMOS transistor will also be surrounded by the N-well region.
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10. Transistor Features

These three steps are identical to the ones done for the NMOS.

1. Draw the gate poly

2. Place the contacts
3. Cover contacts with Metal-1
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11. The P-Select Layer

As with the NMOS transistor, the p-type doping (implantation) window over the active area must be defined using the n-select layer.

1. Select `pselect` layer from the LSW

2. Draw a rectangle that extends over the active area by 0.6\( \mu \) (2 lambda) in all directions.
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12. Drawing the N-Well

In this process, the silicon substrate is originally doped with p-type impurities. NMOS transistors can be realized on this p-type substrate simply by creating n-type diffusion areas. For the PMOS transistors however a different approach must be taken: A larger n-type region (n-well) must be created, which acts like a substrate for the PMOS transistors.

From the process point of view, the n-well is one of the first structures to be formed on the surface during fabrication. Here we chose to draw the n-well after almost everything else is finished. Note that the drawing sequence of different layers in a mask layout is completely arbitrary, it does not have to follow the actual fabrication sequence.

1. Select the \textit{nwell} layer from the LSW

2. Draw a large n-well rectangle extending over the P-Diffusion

The n-well must extend over the PMOS active area by a large margin, at least 1.8u (6 lambda)
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13. Placing the PMOS and NMOS transistors

In this example, we did not pay much attention to the location of the transistors while building them. As long as the design rules are not violated, the transistors can be placed in any arbitrary arrangement. Yet based on our original signal flow diagram, it is more desirable to place the PMOS transistor directly on top of the NMOS transistor- for a more compact layout.

1. Select the PMOS transistor

First make sure that you are in selection mode. If you are in any other mode (like rectangle drawing mode) exit the mode by pressing "ESC". Now using the mouse, click and drag a box that covers your PMOS. If you were successful, all the objects within the PMOS would be highlighted as in the figure below:

2. From the menu Edit select the option Move
( Edit --> Move )
A window will pop-up similar to the copy window. This time we will have to change the Snap Mode option to Anyangle so that we can move the transistor freely.

3. Pick the reference point

We will be asked to find a reference point for the object to be moved. The cursor will practically grab the object from that reference point. Since we want an accurate placement, it is advisable to select a point for which alignment is simpler. The corner between the diffusion and the poly is a good place to grab the PMOS.

After we have picked the reference point, the outline of the shape will appear attached to the cursor and we will be able to move the shape around. Since the minimum distance from diffusion to the n-well edge is 1.8u, the PMOS and NMOS have to be at least 3.6u apart. We can place a ruler to help us aligning the two shapes and to measure the distance.
4. Place the transistor

You can drop the selected object (in this case consisting of the n-well, the p-active, poly and contacts) into its final location by clicking once on the left mouse button.
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14. Connecting the Output

1. Draw a Metal-1 rectangle between NMOS and PMOS drain region contacts

Note that the minimum Metal-1 width is 0.9u (3 lambda), thus narrower than the Metal-1 covering the contacts. Also note that the transistors are completely symmetric, the source and drain regions are interchangeable.
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15. Connecting the Input

The next step will be to connect the gates of both transistors, which will form the input. To do this, we could use the rectangle command again, but this time we will use a different command, the path command. Throughout this tutorial, you will see that you typically have multiple options, commands or procedures available to create the same features in the layout. Please become familiar with as many of such options as possible.

1. Select poly layer from the LSW

2. From the Create menu select Path
   ( Create --> Path )

The path options box will pop up:

In the path mode you can draw lines (or paths) with the selected layer. The width of the drawn line can be adjusted; the default is the minimum width of the selected layer.
3. Start path

To start the path, click on the middle of the PMOS poly extension. You'll see a ghost line appear. Move this ghost line to the NMOS poly extension.

4. Double click to finish path

A single click will finish a line segment and let you continue drawing. A double click will finish the path.
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16. Making a Metal-1 connection for the Input

We have already decided in our signal flow graph that we want the input in Metal-1. Therefore we have to make a connection from the poly layer to the Metal-1 layer.

This connection can be done manually by drawing a poly contact layer between Metal-1 and poly, but we will use the path command to automatically add the contacts.

1. Starting from the poly line connecting the gates, start drawing a horizontal poly path

2. On the Path Options dialog box, click on Change To Layer and switch to Metal1

This will automatically add a contact to the end of the current path. Note that this will still be a ghost line. You can place the contact at a certain location by clicking once, thereafter the path will continue using the new layer.
3. Finish the path

You can finish the path by double clicking. Note that you will not be able to see the contact between the metal and poly layer, there will be a red square instead. This is called an instance. An instance is practically a finished layout that is included completely in your circuit. Since it is a complete layout, it is not possible to edit that layout from within your cell, it is said to be on a lower level of hierarchy.

By default, only the current layer of hierarchy is visible. Objects that you include, as instances will be shown as boxes corresponding to their size. You can press SHIFT-F to see all levels of hierarchy. CTRL-F will return you to viewing only a single layer of hierarchy.
Now that our transistors are placed and connected, we will have to add Power and Ground rails. Usually a layout consists of a large number of cells, all of which need power and ground connections. Therefore it is common to design cells such that they will have one continuous, wide power and ground connection when placed side by side.

Our Signal Flow Graph suggests horizontal power and ground lines in Metal-1.

1. Draw the Power Rail in Metal-1 above the PMOS
2. Draw the Ground Rail in Metal-1 below the NMOS

Make sure to connect the Power Rail and the Ground rail to the source contact of the PMOS and to that of NMOS, respectively.
The substrate on which the transistors are built must be properly biased. The way to do this is to add substrate contacts. The NMOS transistors are built on a p-type substrate, we will have to create a p-type substrate contact.

1. **Draw a P-select square next to the NMOS transistor.**

Since the contact will be made to p-substrate, the contact area will have to be p-type.

2. **Draw a P-active square inside the P-select area.**

This will define the active area of the substrate contact. Make sure that you are not violating any **design rules** associated with active area spacing.
3. Draw the active contact square inside the p-type active area.

4. Make a metal connection to ground, covering the entire substrate contact.
Note that the substrate contact can also be created and placed as an instance, instead of drawing every item separately. This alternative approach will be demonstrated in the next step, for the n-well contact.
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19. N-Substrate Contact

The PMOS transistor was placed within the n-well, this well also has to be biased with the VDD potential. This will be done with an n-type substrate contact.

We can follow the same steps that we did for the p substrate contact, but we will try to introduce another method. Almost all of the interlayer connections are already available as instances in your design library. We used the metal-poly contact instance while connecting the input. Similar instances also exist for the substrate connections.

1. From the menu Create select option Instance
   (Create --> Instance)

This will pop-up the instance options menu.

You'll have to provide a cell name and library here. It may be the case that you already know the cell name and cell view, but in this case it is better to Browse in your library to find the appropriate cell.
This is essentially the same library browser that you access when you start Cadence Design Tools. It lets you choose the library, cell and cell view. Your selection will be transferred to the Instance options menu.

![Library Browser Image]

The N-substrate contact is named NTAP, and only has a *symbolic* view.

2. **Move the instance to the desired location.**

Once you have selected the instance, the cursor will show a ghost image representing the instance, and you'll be able to move the instance to the desired location:

![Instance Movement Image]

3. **Place the instance.**

Once satisfied, you can click to place the instance. You'll remain in the instance mode after you have placed the instance, press "ESC" to go back to selection mode again. Note that in this example, the n-well contact has been placed right on top of the n-well boundary, which will obviously generate a rule violation. The n-well is simply not wide enough to
accommodate both the PMOS transistor and the contact. This will have to be dealt with in the next step.

4. Make the power connection.

The instance will not automatically connect itself to the power supply rail. This connection has to be made by either a Metal-1 rectangle or path.
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20. Enclosing the substrate contact

In the previous step we tried to place the n-type substrate contact in the n-well. Since we had drawn the n-well to cover the P-diffusion at minimum length, the well is not wide enough to accommodate the additional contact. We must enlarge the n-well, so that it also covers the substrate contact.

One way to do this would be to simply draw an adjoining rectangle using the n-well layer. Instead, we will try to modify the existing rectangle, so that it covers the contact.

1. Press F4 on the keyboard to toggle selection mode.

By default, the selection mode will only select whole objects. Pressing "F4" will change this default to partial selection. The information bar will start displaying "(P) Select" (P for partial) instead of "(F) Select" (F for Full).

2. Move cursor over the left edge of the n-well.

You'll notice that as soon as the cursor is close to the edge, only the edge line will be highlighted as a pale dashed line.

3. Click once to select the edge.
3. Move mouse over the selected edge (without pressing any mouse buttons).

You'll notice that the cursor changes shape when you are close to the edge.

4. Press and hold left mouse button when cursor changes above the selected edge.

You have grabbed the edge, and as long as you do not release the mouse button you can "stretch" the edge. Move the edge of the n-well so that all of the substrate contact is covered by n-well.
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21. Design Rule Checking

The layout must be drawn according to strict design rules. After you have finished your
design, an automatic program will check each and every feature in your design against
these design rules and report violations. This process is called Design Rule Checking.

Our design is finished. We must now perform a Design rule Check to see if we have any
errors.

1. From the menu Verify select option DRC
   ( Check --> DRC )

   ![DRC options dialog box]

   This will pop up the DRC options dialog box.

2. Start DRC

   The default options for the DRC are adequate for most situations. DRC results and
   progress will be displayed in the CIW.
You'll have to check the results from the CIW. In this example we have two poly-to-poly contact spacing errors. You can also see that the rule number for this is \( 5.5 \), and the spacing is supposed to be at least 1.5\( \mu \)m

The errors are also highlighted on the layout.

As it is mostly the case, one misplacement will cause multiple DRC errors. The error can be corrected by moving the contact further to the left.
After moving the contact to the left, we will have to perform another DRC.

This is a successful DRC.
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22. Final Layout

This is the completed layout of the CMOS inverter.

Congratulations.