Low-Power CMOS Design
for
NTUEE Advanced VLSI Course

Data source:
2. "Can we simultaneously achieve High Speed and Low Power in IC Design?", by Prof. Wentai Liu, in 7th VLSI/CAD Symposium, 1996.
3. Chap. 16 of Textbook.
Low Power Design - An Emerging Discipline

1. Historical figure of merit for VLSI design - performance (circuit speed) and chip area (circuit density). But

2. Power dissipation is now an important metric in VLSI design.
   (a) No single major source for power savings across all design levels - Required a new way of THINKING !!!
   (b) Companies lack the basic power conscious culture and designers need to be educated in this respect.

3. Overall Goal - To reduce power dissipation but maintaining adequate performance.
## Motivation - Microprocessor

<table>
<thead>
<tr>
<th>Processor</th>
<th>Source</th>
<th>Date (ship)</th>
<th>Bits (i/d)</th>
<th>Clock (MHz)</th>
<th>SPEC-92 int</th>
<th>SPEC-92 fp</th>
<th>SPEC-95 int</th>
<th>SPEC-95 fp</th>
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<th>Power (W) peak/typ</th>
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1. Battery Powered Systems - Extended Battery Life and reduce weight and size

2. High Performance Systems
   (a) Cost
      i. Packaging (chip carrier, heat sink, card slots, plenum, ...)
      ii. Power Systems (supplies, distribution, regulators, ...)
      iii. Fans (noise, power, reliability, area, ...)
      iv. Operating cost to customer - Energy Star issue
   (b) Reliability
      i. Failure rate increase by 4X for $T_j \; @ \; 110^\circ C \; vs \; 70^\circ C$
      ii. Mission critical operation, 100
   (c) Size and Weight - Product footprint (office and deskspace)
The Power Crisis: Portability

- Multimedia Terminals
- Laptop Computers
- Digital Cellular Telephony

Expected Battery Lifetime increase over next 5 years: 30-40%
A Multi-Media Terminal - The Infopad

- Present day battery technology - 20 lbs for 10hrs.
IC Design Space

- Speed
- Area
- Complexity
- Power
Low Power Design

- Sources of power dissipation:

\[ P = P_{\text{switching}} + P_{\text{short-circuit}} + P_{\text{leakage}} + P_{\text{static}} \]

Definitions:

- Switching power \( P = CV^2 f \cdot \alpha \)
- Short circuit power \( P = I_{\text{sc}} V \)
- Leakage power \( P = I_{\text{leakage}} V \)
- Static power \( P = I_{\text{static}} V \)

\( \alpha \): switching activity factor

Low power design would look at the trade-offs of the above issues
Dynamic Power Consumption

Energy/transition = \( C_L \times V_{dd}^2 \)

Power = Energy/transition \( \times f \) = \( C_L \times V_{dd}^2 \times f \)

- Not a function of transistor sizes!
- Need to reduce \( C_L \), \( V_{dd} \), and \( f \) to reduce power.
- Reduce the Probability, \( P_o \rightarrow 1 \)
Dynamic Power Consumption - Extended

Power = Energy/transition * transition rate

\[ = C_L \times V_{dd}^2 \times f_{0\rightarrow1} \]

\[ = C_L \times V_{dd}^2 \times P_{0\rightarrow1} \times f \]

\[ = C_{EFF} \times V_{dd}^2 \times f \]

Power Dissipation is Data Dependent
Function of Switching Activity

\[ C_{EFF} = \text{Effective Capacitance} = C_L \times P_{0\rightarrow1} \]
Ultra Low Power System Design

Power minimization approaches:
- Run at minimum allowable voltage
- Minimize effective switching capacitance

System
- Partitioning, Power-down

Algorithm
- Complexity, Concurrency

Architecture
- Parallelism, Pipelining, Redundancy

Circuit/Logic
- Sizing, Logic Styles, Logic Design

Technology
- Threshold Reduction
1. Progress in SOI and bulk silicon
   (a) 0.5V operation of ICs using SOI technology
   (b) 0.9V operation of bulk silicon memory, logic, and processors

2. Increasing densities and clock frequencies have pushed the power up even with reduce power supply.
Delay constraint:

The "best" logic style minimizes power-delay for a given

Power-delay product improves as voltage decreases.

![Graph showing power-delay product vs. delay for different logic styles.]

Choice of logic style
Example: Static 2 Input NOR Gate

Assume:
\[
P(A=1) = 1/2 \\
P(B=1) = 1/2
\]

Then:
\[
P(\text{Out}=1) = 1/4 \\
P(0 \rightarrow 1) = P(\text{Out}=0).P(\text{Out}=1)
\]

\[
= 3/4 \times 1/4 = 3/16
\]

\[C_{\text{EFF}} = 3/16 \times C_L\]

Truth Table of 2 input NOR gate

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<th>Out</th>
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Transition Probability of 2-input NOR Gate

as a function of input probabilities
Switching Activity ($\alpha$):

Example

Due to correlation

Chapter 17
Glitching in Static CMOS

also called: dynamic hazards

A

B

X

C

Z

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<tr>
<td>Z</td>
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Unit Delay
At the Datapath Level...

Tree vs. Chain

(A + B) + (C + D)

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- Can be reduced by reducing the logic depth and balancing signal paths.
Balancing Operations

Example: Addition
Carry Ripple

Transitions due to carry propagation

Chapter 17
Data Representation

Two’s Complement

- Sign-extension activity significantly reduced using sign-magnitude representation
Data coding representation

Binary Vs. Grey coding

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<th>Decimal Value</th>
<th>Binary Code</th>
<th>Grey Code</th>
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<td>15</td>
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Resource Sharing Can Increase Activity

Number of Bus Transitions Per Cycle

\[ = 2 \left(1 + \frac{1}{2} + \frac{1}{4} + \ldots\right) = 4 \]
Resource Sharing Can Increase Activity

Adder1

Adder2

Adder

Transition Probability

Adder (Average per Addition)

Sum Output Bit #
Operating at the lowest possible voltage

- Desire to operate at lowest possible speeds (using low supply voltages).
- Use Architecture optimization to compensate for slower operation.

Approach: Trade-off AREA for lower POWER
Reducing $V_{dd}$

\[ P \times t_d = E_t = C_L \times V_{dd}^2 \]

\[ \frac{E(V_{dd}=2)}{E(V_{dd}=5)} = \frac{(C_L) \times (2)^2}{(C_L) \times (5)^2} \]

\[ E(V_{dd}=2) \approx 0.16 \times E(V_{dd}=5) \]

- Strong function of voltage ($V^2$ dependence).
- Relatively independent of logic function and style.
- Power Delay Product Improves with lowering $V_{DD}$. 
Lowering $V_{dd}$ Increases Delay

\[ T_d = \frac{C_L \cdot V_{dd}}{I} \]

$I \sim (V_{dd} - V_t)^2$

\[ \frac{T_d(V_{dd=2})}{T_d(V_{dd=5})} = \frac{(2) \cdot (5 - 0.7)^2}{(5) \cdot (2 - 0.7)^2} \approx 4 \]

- Relatively independent of logic function and style.
Architecture Trade-offs: Reference Data Path

Critical path delay $\Rightarrow T_{\text{adder}} + T_{\text{comparator}} (= 25\text{ns})$

$\Rightarrow f_{\text{ref}} = 40\text{Mhz}$

Total capacitance being switched = $C_{\text{ref}}$

$V_{\text{dd}} = V_{\text{ref}} = 5\text{V}$

Power for reference datapath = $P_{\text{ref}} = C_{\text{ref}} V_{\text{ref}}^2 f_{\text{ref}}$

Area = 636 x 833 $\mu^2$
- The clock rate can be reduced by half with the same throughput \( \Rightarrow f_{\text{par}} = f_{\text{ref}} / 2 \)
- \( V_{\text{par}} = V_{\text{ref}} / 1.7, \ C_{\text{par}} = 2.15C_{\text{ref}} \)
- \( P_{\text{par}} = (2.15C_{\text{ref}}) (V_{\text{ref}}/1.7)^2 (t_{\text{ref}}/2) \approx 0.36 P_{\text{ref}} \)
Pipelined Data Path

- \( f_{pipe} = f_{ref} \)
- \( C_{pipe} = 1.1C_{ref} \)
- \( V_{pipe} = V_{ref}/1.7 \)

- Voltage can be dropped while maintaining the original throughput.

- \( P_{pipe} = C_{pipe} V_{pipe}^2 f_{pipe} = (1.1C_{ref}) (V_{ref}/1.7)^2 f_{ref} = 0.37 P_{ref} \)
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<th>Architecture type</th>
<th>Simple datapath (no pipelining or parallelism)</th>
<th>Pipelined datapath</th>
<th>Parallel datapath</th>
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A Simple Data Path: Summary
### Computational Complexity of DCT Algorithms

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<th>Additions (8x8)</th>
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<td>Row-Col DCT</td>
<td>1024</td>
<td>1024</td>
<td>Bell core (16x16)</td>
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<tr>
<td>Chen’s Algorithm</td>
<td>256</td>
<td>416</td>
<td>Telettra</td>
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<tr>
<td>Lee’s Algorithm</td>
<td>192</td>
<td>464</td>
<td>SGS - Thompson</td>
</tr>
<tr>
<td>Feig’s Algorithm (scaled DCT)</td>
<td>54</td>
<td>462</td>
<td>IBM (GP computer)</td>
</tr>
</tbody>
</table>

- Reducing # of operations (switching events) is important in reducing the power.
- Routing and layout issues for irregular structures vs. regular structures.
Power Down Techniques

Operating States

ACTIVE OR FULL-ON (FASTEST CLOCK)

STANDBY (SLOW CLOCK)

SUSPEND OR SLEEP (SLOWEST CLOCK or SHUT DOWN)

Activity Monitor
1. Potential for power reduction via software modification is relatively unexploited.

2. Code size and algorithmic efficiency can significantly affect energy dissipation

3. Examples -
   

Power Hunger - Clock Network (Always Ticking)

1. H-Tree - design deficiencies based on Elmore delay model

2. PLL - every designer (digital or analog) should have the knowledge of PLL
   - multiple frequencies in chips/systems - by PLL
   - Low main frequency, But
   - Jitter and Noise, Gain and Bandwidth, Pull-in and Lock Time, Stability ...

3. Local time zone

4. Self-Timed

5. Asynchronous

⇒ Use Gated Clocks, Sleep Mode
Power Analysis in the Design Flow

Too Little

\[ Z = X \times Y \]
if \((Z < 0)\) then \(Z = 0\)

Algorithm

Fast & Accurate

Architecture

Too Late

Gate/Circuit

Exploration

- Power
- Time
- Area
Human Wearable Computing - Power

- Wearable computing - embedding computer into clothing or creating a form that can be used like clothing.
- Current computations are limited by battery capacity, output current, and electrical outlet for recharging

---

Conclusions

1. High speed design is a requirement for many applications
2. Low power design is also a requirement and an emerging discipline
3. A new way of THINKING to simultaneously achieve both!!!
4. Low power impacts on the cost, size, weight, performance, and reliability
5. A universal Vdd is a trend
6. CAD tools high level power estimation and management
7. Don't just work on VLSI, pay attention to MEMS - lot of problems and potential is great
Future Work

1. Portable Multimedia Terminal
2. Wireless C&C
3. System on Chip (From Dr. Yang of Windbond)
Wireless Computing/Communication

Fiber Optic Backbone > 10 Gbits/sec

- COMPUTE SERVERS
- WIRELESS BASE STATION
- VIDEO DATABASE
  Compressed Video
- SPEECH RECOGNITION
- LARGE COMMERCIAL DATABASE
  Airline schedule, Newspaper, ...
- PERSONAL COMMUNICATORS
  InfoPad (A Portable Multimedia Terminal)
  - Speech I/O and Pen Input
  - X-terminal
  - Full-motion Video

Future Work
A Portable Multimedia Terminal

Antenna ↔ Radio Modem

Protocol Module (2mW)

Pen Digitizer
Speech Codec
Text/Graphics Frame-Buffer Module (1mW)

Video Decompression Module (2mW)

Protocol, ECC, Buffering, Video Decompression, and I/O

Future Work
### III. System Value of IC Product

- **Concept of lays**

<table>
<thead>
<tr>
<th></th>
<th>Circuit</th>
<th>Device</th>
<th>Process Module</th>
<th>Equipment</th>
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<tr>
<td>Software</td>
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IC → System

Future Work

第5張 44
IV. System on Chip

- Entire system function
  - Logic + Memory
  - More than two types of devices

- Allow more freedom in architecture

- Cost/Performance trade-off
V. New Opportunity for Taiwan IC Industry

PAST

- Digital IC
- μP
- IBM Compatible + MD-DOS

FUTURE

- System - On - Chip
  - Reduce head-on competition on standard products
  - Technology will be available
  - Manufacturing Service available
  - Same starting point as other countries
  - Can have more R/D focus

Future Work