Digital system Design Homework #4
Deadline:2004/5/14

Objective: design a simple state machine

☐ In this homework, you will write a simple state machine in Verilog. You can choose the topic freely.
Examples:
- Traffic light signal controller at crossroads
- Automatic vending machine
- Automatic teller machine
- Other state machine topics…

☐ Draw the state transition diagram of your state machine.
☐ Write Verilog code to implement the state machine.
☐ Write a testbench to verify that your state machine is correct. Try to verify all different paths in your state transition diagram.
☐ (optional) In course materials, there are 3 different coding styles for a same state machine. Try to use a different coding style to implement your design and verify it.

Submission list:(hardcopy only)
  a. State transition diagram of your design
  b. Verilog code of state machine
  c. testbench
  d. List the problems you met and solutions.