Problem 1: (23 points)

(a) This circuit is actually J-K flip flop, so it is stable and with the state transition table as following.

<table>
<thead>
<tr>
<th>$X_0$</th>
<th>$X_1$</th>
<th>$Q_1$</th>
<th>$Q_1^+$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

1. Stable (1%)
2. State transition table (4%)

(b) Miss one value -0.5 %, total 5 %.

(c) Negative edge trigger for 2 %. Miss one value -0.5 %, total 8 %.

Problem 2: (10 points)

1. State transition graph (2%) (minor mistake -1%)
2. SOP of $Q_2Q_1Q_0$ and $z$ (2%*4, minor mistake -1%)
3. Two kinds of solution will be ok, but state transition graph should be corresponding to SOP (state graph contradict with SOP, -1%)
$D_2 = x + Q_2 Q_0 + Q_2 Q_1$
$D_1 = x + Q_2 Q_1 Q'_0 + Q_1 Q_0$
$D_0 = x + Q_2 Q'_0 + Q_1 Q_0'$
$z = Q'_2 Q'_1 Q'_0$

$D_2 = x Q_2 + x Q_1 + x Q_0 + Q_2 Q_0 + Q_2 Q_1$
$D_1 = x Q_1 + x Q_0 + Q_2 Q'_1 Q'_0 + Q_1 Q_0$
$D_0 = x Q_0 + Q_2 Q'_0 + Q_1 Q_0'$
$z = Q'_2 Q'_1 Q'_0$

**Problem 3: (17 points)**

*<Solution>*

(a) Mealy machine
(b) let $S_0=00$ $S_1=01$ $S_2=11$ $S_3=10$

<table>
<thead>
<tr>
<th>$X_1X_2$</th>
<th>$Q_1Q_2$</th>
<th>$Q_1^+Q_2^+$</th>
<th>$Z$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>00</td>
<td>00</td>
<td>11</td>
</tr>
<tr>
<td>$S_0$</td>
<td>00</td>
<td>00</td>
<td>11</td>
</tr>
<tr>
<td>$S_1$</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>$S_2$</td>
<td>11</td>
<td>10</td>
<td>00</td>
</tr>
<tr>
<td>$S_3$</td>
<td>11</td>
<td>10</td>
<td>01</td>
</tr>
</tbody>
</table>

(c) $t_{clk} = t_x + t_c + t_{su} = 0.5t_{clk} + 7 + 2$

$t_{clk} = 9 \times 2 = 18$ ns

**Problem 4: (10 points)**

**Solution**

**Problem 5: (24 points)**
(a) (5%) What is the set of input sequences recognized by the state graph when the initial state is A? (Supposed that the input sequence length ≤ 6)

\{0001, 001-, 0110, 110, 1--110\}
\{001, 001-, 0110\} 写错扣一分，\{110\} 写错扣一分，\{1--110\} 写错扣一分

(b) {0001, 001-, 0110, 110, 1--110}
\{0001, 001-, 0110\} 写错扣一分，\{110\} 写错扣一分，\{1--110\} 写错扣一分

(c) (5%) What is the set of input sequences recognized by the state graph when the initial state is C? (Supposed that the input sequence length ≤ 6)

\{10, --0001, --001-, --0110, --110\}
\{10\} 写错扣一分，\{--0001, --001-, --0110\} 写错扣一分，\{--110\} 写错扣一分

(d) (2%) Derive a minimum-length input sequence that distinguishes states A and C. That is, state A and state C as initial states should produce different outputs at the end of the input sequence.

\{10\} 没写出\{10\} 扣两分，多写其他一个扣一分

(e) (5%) Minimize the state graph by identifying and merging equivalent states.

(C = E), (F = J), (G = K) · 少merge一个扣两分，扣到五分为止

(f) (2%) To implement the minimized state graph using a ROM, what is the minimum size of the ROM in term of the number of words and the word size?

1 input, one output, 3 state variables for 8 states.
number of words = 2^(1+3) = 16
word size = 1+3 = 4
写错一个扣一分

(g) (5%) Draw the state graph of an equivalent Moore machine with state minimized.
畫錯一個地方扣一分，扣到五分為止

**Problem 6: (6 points)**

No, it can’t be implemented by an iterative circuit.
It’s because \( y_i \) value can not be determined only with the information of \( x_0 \) to \( x_i \).
The value of \( y_i \) is actually depends on \( x_i \) to \( x_n \).
回答 Yes 不給分，有回答 No 沒說出關鍵原因扣四分

**Problem 7: (10 points)**

<Solution>

(a)

<table>
<thead>
<tr>
<th>State</th>
<th>9-Bit Value in Product Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S_1 )</td>
<td>000001011</td>
</tr>
<tr>
<td>( S_2 )</td>
<td>01101011</td>
</tr>
<tr>
<td>( S_3 )</td>
<td>011101101</td>
</tr>
<tr>
<td>( S_4 )</td>
<td>100111101</td>
</tr>
</tbody>
</table>

Right answer for 5 %.
Wrong answer, but previous state values are correct for 3 %.(each state is 1%)
Wrong answer without procedure for 0%

**Problem 8: (bonus 5 points): Verilog HDL – Code Debugging**

<Solution>

```verilog
module 4x1MUX(Z,D0,D1,D2,D3,S0,S1); (1.0pts) 分號結尾
   (1.0pts) 命名開頭必須為大小寫字母或底線(_)
input D0,D1,D2,D3,S0,S1;
output Z;
wire Z; (1.0pts) 刪掉
```
wire T0, T1, T2, T3, S0_, S1_;

/* Structural Modeling*/(1.0pts) 少*/必須補上
and (T0,D0,S0_,S1_),
    (T1,D1,S0_,S1),
    (T2,D2,S0,S1_),
    (T3,D3,S0,S1);
not (S0_,S0), (S1_,S1);
or (Z,T0,T1,T2,T3);
Endmodule (1.0pts)e 小寫