6.2. Memory Device (Chapter 11 of Textbook)

- Latch = set-reset latch
- Flip-flop = a latch with clock

Timing diagram:

(a) Set

(b) Reset

(c) Clock

6.3.1. Latches

\[
\begin{align*}
\begin{array}{c}
\text{S} \\
\text{Q} \\
\text{Q'}
\end{array} & \quad \begin{array}{c}
\text{0} \\
\text{0} \\
\text{1}
\end{array} & \quad \begin{array}{c}
\text{0} \\
\text{1} \\
\text{0}
\end{array} & \quad \begin{array}{c}
\text{1} \\
\text{0} \\
\text{0}
\end{array}
\end{align*}
\]

(a) Set latch

Set-reset latch (SR latch) = NOR structure

\[
\begin{align*}
\begin{array}{c}
\text{SR} \\
\text{Latch}
\end{array} & \quad \begin{array}{c}
\text{NOR} \\
\text{SR}
\end{array}
\end{align*}
\]
(II) NAND SR latch (Active low)

- Excitation table

<table>
<thead>
<tr>
<th>Excitation Input</th>
<th>Present State</th>
<th>Next State $\bar{Q}^*$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>0</td>
<td>0, no change</td>
</tr>
<tr>
<td>0 1</td>
<td>0</td>
<td>Reset</td>
</tr>
<tr>
<td>1 0</td>
<td>1</td>
<td>Set</td>
</tr>
<tr>
<td>1 1</td>
<td>X</td>
<td>Not allowed, unstable state(s)</td>
</tr>
</tbody>
</table>

- State diagram

-K-map of latch output $\bar{Q}^*$ (next state)

$\bar{Q}^* = S + R\bar{Q}$

Characteristic equation of the SR latch:

\[
\begin{align*}
\text{(II) Case 1: } & S = R = 0, \quad \bar{Q}^* = \bar{Q} \quad (\text{State unchanged}) \\
\text{(II) Case 2: } & S = 1, R = 0, \quad \bar{Q}^* = 1, \quad (\text{Set operation}) \\
\text{(II) Case 3: } & S = 0, R = 1, \quad \bar{Q}^* = 0, \quad (\text{Reset operation})
\end{align*}
\]
6.7.2. Gated SR latch

- Excitation table
- State diagram

6.7.3. Delay latch (D-latch)

- Characteristic Equation: $Q^* = SCR \bar{Q} + \bar{C}A$

Figure 6.11 Gated SR latch characteristics. (a) Excitation table. (b) State diagram.

Figure 6.15 Delay latch (D-latch). (a) Logic symbol. (b) NAND implementation. (c) NOR implementation.

<table>
<thead>
<tr>
<th>Enable input</th>
<th>Excitation input</th>
<th>Present state</th>
<th>Next state $Q^*$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>x</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
characteristic equation:
\[ q^* = SC + R \bar{Q} + \bar{C} \bar{Q} \] (gated SR latch)
\[ = D \bar{C} + (\bar{S}) \bar{Q} + \bar{C} \bar{Q} \]
\[ = D \bar{C} + \bar{Q} \bar{C} + \bar{Q} \]
\[ = D \bar{C} + \bar{Q} \]

Timing diagram (Fig. 6.17)

Figure 6.17: D Latch Timing Diagram

-TTL: 7475, 74116

* 6.4. Flip-flops:
- For synchronous sequential logic
- Use a control signal called "clock" to restrict the time at which the states may change.

- 6.4.1. Master-slave SR FF.
  \[ S = 0, \text{master in gated mode, slave in hold mode} \]
  \[ S = 1, \text{slave in } = , \text{master in enabled} \]
- Timing diagram

Figure 6.21 Master-slave SR flip-flop. (a) Logic diagram. (b) Pulse-triggered device logic symbol. (c) Timing behavior. (d) Timing constraints

- Excitation table and state diagram

Figure 6.22 SR master-slave flip-flop characteristics. (a) Excitation table. (b) State diagram.

- pulse-triggered flip-flop
6.4.1. Master-Slave SR Flip-Flop

6.4.3. Master-Slave JK Flip-Flops

- S=R=1 is not allowed in SR latch
- S J= S (Jump), J= K=1, \( Q^t = \overline{Q} \) (preset)
  K= R (clear), J= K=1, \( Q^t = \overline{Q} \) (reset)
- Excitation table

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>C</th>
<th>Q*</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

- JK edge-triggered D flip-flop

- Pulse-triggered DFF requires both rising and falling edges of the clock.

- Positive edge triggered  

- Negative edge triggered  

- Excitation table

- Inputs | Outputs |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>J</td>
<td>L</td>
</tr>
<tr>
<td>K</td>
<td>H</td>
</tr>
<tr>
<td>C</td>
<td>H</td>
</tr>
</tbody>
</table>

- Mode

- Set

- Clear

- Not allowed

- Clock is not held

- Hold
- Edge-triggered JK flip-flop
- Edge-triggered T flip-flop (J=K=1)

\[
\begin{array}{c}
\text{PRE} \\
\hline \\
T \rightarrow 0, \quad \bar{Q}^+ = Q \quad \text{(unchanged)} \\
T = 1, \quad \bar{Q}^+ = \bar{Q} \quad \text{(toggled)} \\
\end{array}
\]

**Characteristic Equations (next-state) for Flip-Flop**

1. \( Q^+ = S + RQ \) \((SR=0)\) \((S-R Flip-Flop)\)
2. \( Q^+ = T \oplus Q = T\bar{Q}^* + \bar{T}Q^* \) \((T Flip-Flop)\)
3. \( Q^+ = J\bar{Q}^* + KQ^* \) \((J-K Flip-Flop)\)
4. \( Q^+ = D \) \((D Flip-Flop)\)

For SR type, \( S=R=1 \) is forbidden.