Access IC Design and Implementation

報告人: 台大電子所吳安宇副教授
Office：EE 電二 R409
Lab：EE 電二 R331
E-mail：andywu@cc.ee.ntu.edu.tw
URL：http://access.ee.ntu.edu.tw

For New ICS MS Students on May 14, 2004
Information ACCESS

❖ **Access Systems:**
  ❖ Digital Subscriber Loops (DSL)
    ➢ Asymmetric DSL (ADSL) and Very-high-speed DSL (VDSL)
    ➢ High-speed DSL (HDSL)
    ➢ Single-pair HDSL (SHDSL/HDSL2)
  ❖ Gigabit (1000base-T) and 10G Ethernet
  ❖ Digital Audio/Video Broadcast (DAB/DVB)
  ❖ Wireless LAN and Broadband Wireless Access (BWA)

❖ **Research Focus:** Develop state-of-the-art DSP/VLSI algorithms/architectures/circuits for Access Systems
Communication Block Diagram

MPEG, JPEG

Access Engine

Encryption \rightarrow Channel Coding \rightarrow Modulation

Decryption \rightarrow Channel Decoding \rightarrow Demodulation

Information Source \rightarrow Source Encoding

Information Destination \rightarrow Source Decoding
Focused Project: Reconfigurable Communication Engine
I. Reconfigurable Multi-mode RS Architecture

- Reed Solomon code is currently adopted as channel coding schemes in many communication systems.

<table>
<thead>
<tr>
<th>Application</th>
<th>Specification: $RS(n,k,t)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDD</td>
<td>$RS(72,64,4)$</td>
</tr>
<tr>
<td>CD</td>
<td>$RS(32,28,2)$</td>
</tr>
<tr>
<td>DVD</td>
<td>$RS(208,192,8)$</td>
</tr>
<tr>
<td>DVB</td>
<td>$RS(204,188,8)$</td>
</tr>
<tr>
<td>CCSDS</td>
<td>$RS(15\sim255,n-16,8)$</td>
</tr>
<tr>
<td>xDSL &amp; Cable modem</td>
<td>$RS(\sim255,n-t, t = 1\sim8)$</td>
</tr>
</tbody>
</table>

- Various applications with different $RS(n,k,t)$ specifications
  - Several silicon IP are required
  - High design complexity and re-design effort
# II. FEC Specification in CDMA2000

- Two modes:
  - **Convolutional code** with multi-spec \((1/2, 1/3, 1/4)\)
  - **Turbo code**

<table>
<thead>
<tr>
<th>Channel Type</th>
<th>Forward Error Correction code</th>
<th>Code Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Access Channel</td>
<td>Convolutional</td>
<td>1/3</td>
</tr>
<tr>
<td>Enhanced Access Channel</td>
<td>Convolutional</td>
<td>1/4</td>
</tr>
<tr>
<td>Reverse Common Control Channel</td>
<td>Convolutional</td>
<td>1/4</td>
</tr>
<tr>
<td>Reverse Dedicated Control Channel</td>
<td>Convolutional</td>
<td>1/4</td>
</tr>
<tr>
<td>Reverse Fundamental Channel</td>
<td>Convolutional</td>
<td>1/2, 1/3, 1/4</td>
</tr>
<tr>
<td>Reverse Supplemental Code Channel</td>
<td>Convolutional or Turbo code</td>
<td>1/2, 1/3, 1/4</td>
</tr>
</tbody>
</table>

pp. 6
### III. Programmable 64~2048 Point FFT/IFFT Processor

- **OFDM Applications and FFT Specification**

<table>
<thead>
<tr>
<th>Application</th>
<th>FFT Size</th>
<th>$T_{FFT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>WLAN</td>
<td>64</td>
<td>3.2 $\mu$s</td>
</tr>
<tr>
<td>ADSL</td>
<td>2x256</td>
<td>231 $\mu$s</td>
</tr>
<tr>
<td>VDSL</td>
<td>2x256x2^n, n=0:4</td>
<td>231 $\mu$s</td>
</tr>
<tr>
<td>DAB</td>
<td>256x2^n, n=0:3</td>
<td>31x2^n $\mu$s, n=0:3</td>
</tr>
<tr>
<td>DVB-T</td>
<td>2048/8192</td>
<td>224/896 $\mu$s</td>
</tr>
</tbody>
</table>
Proposed Programmable 64~2048 point FFT Processor Architecture
Reconfigurable Silicon Intellectual Property (SIP)
Designs for Next-Generation Communication Systems

I. Reconfigurable Reed Solomon Decoder for Multi-Mode Communication Systems

II. Dual-mode Turbo/Convolutional Decoder for 3G Wireless Communications

III. Programmable FFT Processor for OFDM Systems
Mobile Reception of *Digital Video Broadcasting- Terrestrial (DVB-T)*

- Extensively tested throughout Germany:
  - DVB-T received successfully at 275 km/h.
  - Commuters watched DVB-T on trams
- A convincing demonstration of the robustness of DVB-T
- An opportunity for high-speed data transmission on the move
**Ongoing Project:** Platform-based SOC Design for Multi-mode DVB-T Baseband Receiver
Platform-based Design: 802.11i Security System

- **Application Layer**: SSL
  - **SSL**: Secure Socket layer

- **Transport Layer (TCP, UDP)**

- **Network Layer (IP)**: IPSec
  - **IPSec**: IP Security

- **802.11 Link. Layer**
  - Robust Security Network
    - **WEP or AES**: WEP or AES
      - **WEP**: Wired Equivalent Privacy
      - **AES**: Advanced Encryption Standard

**Our Focus**

802.11 Phys. Layer
Advanced Encryption Standard (AES) Silicon IP

ARM CPU Platform-based Design for WLAN Security System
Participated Projects (I)

- 國科會「IT整合科技計畫」
  - (90-92): High-performance Digital IP module designs for xDSL Systems (FFT, Viterbi, Reed Solomon codec)
  - (93-95): Platform-based design for Wireless LAN Security System

- 聯發科技
  - (91-92): Turbo Codec IC design for Wireless Systems
  - (93-94): Polar Transmitter Design for 2G/2.5G Wireless Systems

- 威盛電子
  - (90-92): Gigabit Ethernet (GbE) LAN transceiver IC Design: Baseband DSP System.
Participated Projects (II)

- 国科会三年群計畫 (92-95): 多媒體通訊系統中可重組化運算技術之研究
  - Reconfigurable Communications Engine, including Feedforward Error Correction (FEC) cores and Modulation (Single-carrier and multi-carrier) Core

- 国科会「前瞻系統晶片研究計畫」 (92-95): 百億位元的乙太網路系統晶片設計
  - High-speed DSP algorithms and architectures for 10G Ethernet Optical transmission Systems

- 国科会「3C整合科技計畫」 (92-95): 室內用寬頻無線資訊接取系統
  - Encryption/decryption Engine (e.g., RSA, EC AES) for Wireless/Embedded Communication System
Some Student Awards

- 2004國家晶片系統設計中心「優良晶片」設計（獲獎學生：許槐益，設計名稱：適用於高速通訊系統之可規劃多模式里德所羅門編解碼模組）。

- 第一屆全國SOC系統晶片設計比賽
  - 軟硬體發展平台組 優等獎 (題目:Digital Frame)
  - SoC晶片組 優等獎 (題目:DVB-T Baseband Receiver Design)

- 教育部/國科會主辦大專院校矽智產Silicon Intellectual Property (SIP) 設計競賽：
  - 90學年度Soft IP組 佳作 (題目：Turbo Codec IP for Communication Systems)
  - 91學年度Soft IP不定題組 佳作 (題目：第三代行動通訊雙模式維特比/渦輪碼解碼器矽智產設計)
  - Hard IP不定題組 優等 (題目：適用於各式高速通訊系統之可規劃里德所羅得門矽智產設計)

- 91年「沈文仁教授紀念獎」 (獲獎學生:吳政勳，論文名稱：Modified Vector Rotational CORDIC (MVR-CORDIC) Algorithm and Architecture)
Access Lab Profile

- Location: EE building II (Rm. 331, 17坪)

- Manpower:
  - 7 Ph.D. students (2 Phd3, 2 Phd2, 3 PhD1)
  - 6 MS2 students + 7 MS1 students + 2 Part-time MS students
  - 18 Undergraduate project students

- Equipment:
  - 2 Sun Blade 2000 Workstations
  - 2 Sun Ultra 60 Workstations
  - 22 PC and 5 Notebooks for students
Suggested Background

- **Good background but Optional:**
  - Digital Signal Processing
  - Signals and Systems
  - Logic Design
  - Computer Organization
  - VLSI Design and Lab
  - Digital Communications and related courses

- **Required:**
  - *Self-motivated* (very important!)
  - *Disciplined and Innovative* (As an Engineer Requirement!)
Thanks for your attention!!

If you are interested, please check our Homepage
http://access.ee.ntu.edu.tw